NEC

MOS INTEGRATED CIRCUIT
μPD431000A

1M-BIT CMOS STATIC RAM
128K-WORD BY 8-BIT

Description

The μPD431000A is a high speed, low power, and 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The μPD431000A has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available. In addition to this, A and B versions are low voltage operations.

The μPD431000A is packed in 32-pin PLASTIC DIP, 32-pin PLASTIC SOP and 32-pin PLASTIC TSOP (I) (8 × 13.4 mm) and (8 × 20 mm).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (A version: V_{CC} = 3.0 to 5.5 V, B version: V_{CC} = 2.7 to 5.5 V)
- Operating ambient temperature: T_A = 0 to 70 °C
- Low V_{CC} data retention: 2.0 V (MIN.)
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

	Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
					At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.) Note1
	μPD431000A-xxL	70, 85	4.5 to 5.5	0 to 70	70	100	15
	μPD431000A-xxLL					20	3
	μPD431000A-Axx	70 Note2, 100	3.0 to 5.5		35 Note3	13 Note5	
★	μPD431000A-Bxx	70 Note2, 100, 120, 150	2.7 to 5.5		30 Note4	11 Note6	

Notes 1. $T_A \leq 40$ °C

2. V_{CC} = 4.5 to 5.5 V

3. 70 mA (V_{CC} > 3.6 V)

4. 70 mA (V_{CC} > 3.3 V)

5. 20 μA (V_{CC} > 3.6 V)

6. 20 μA (V_{CC} > 3.3 V)

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The mark ★ shows major revised points.

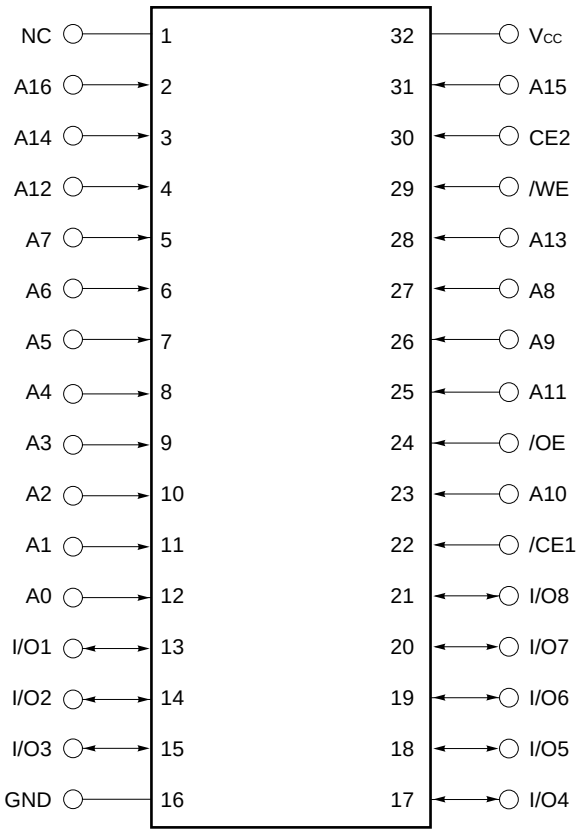
Ordering Information

	Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
	μPD431000ACZ-70L	32-pin PLASTIC DIP (15.24mm (600))	70	4.5 to 5.5	0 to 70	L version
	μPD431000ACZ-85L		85			
	μPD431000ACZ-70LL		70			LL version
	μPD431000ACZ-85LL		85			
	μPD431000AGW-70L	32-pin PLASTIC SOP (13.34 mm (525))	70	4.5 to 5.5		L version
	μPD431000AGW-85L		85			
	μPD431000AGW-70LL		70			LL version
	μPD431000AGW-85LL		85			
	μPD431000AGW-A10		100	3.0 to 5.5		A version
	μPD431000AGW-B12		120	2.7 to 5.5		B version
	μPD431000AGW-B15		150			
	μPD431000AGZ-85L-KJH	32-pin PLASTIC TSOP(I) (8x20) (Normal bent)	85	4.5 to 5.5		L version
	μPD431000AGZ-70LL-KJH		70			LL version
	μPD431000AGZ-85LL-KJH		85			
★	μPD431000AGZ-B10-KJH		100	2.7 to 5.5		B version
	μPD431000AGZ-B15-KJH		150			
	μPD431000AGZ-70LL-KKH	32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)	70	4.5 to 5.5		LL version
	μPD431000AGZ-B15-KKH		150	2.7 to 5.5		B version
★	μPD431000AGU-B10-9JH	32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent)	100	2.7 to 5.5		B version
	μPD431000AGU-B12-9JH		120			
	μPD431000AGU-B15-9JH		150			
★	μPD431000AGU-B10-9KH	32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)	100			

Pin Configurations (Marking Side)

/xxx indicates active low signal.

32-pin PLASTIC DIP (15.24 mm (600))
[μPD431000ACZ-xxL]
[μPD431000ACZ-xxLL]



A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

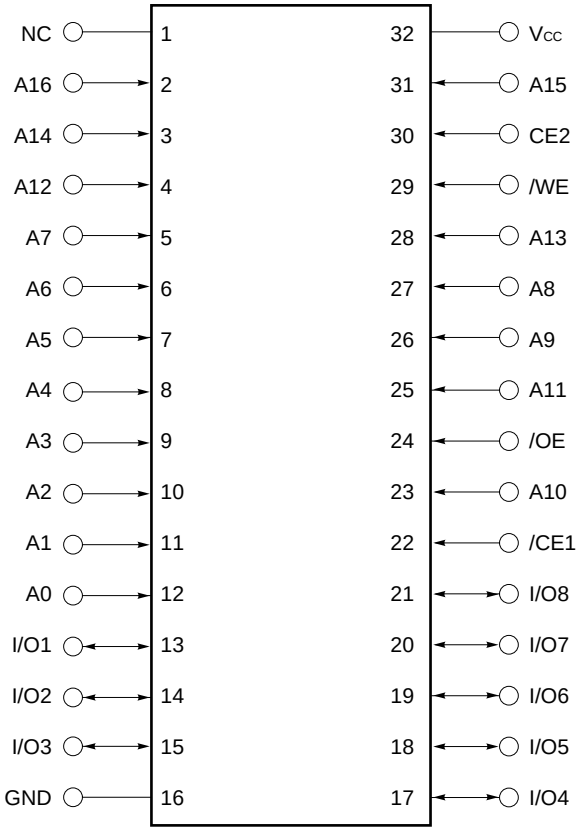
32-pin PLASTIC SOP (13.34 mm (525))

[μPD431000AGW-xxL]

[μPD431000AGW-xxLL]

[μPD431000AGW-Axx]

[μPD431000AGW-Bxx]



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/WE	:	Write Enable
/OE	:	Output Enable
V_{CC}	:	Power supply
GND	:	Ground
NC	:	No connection

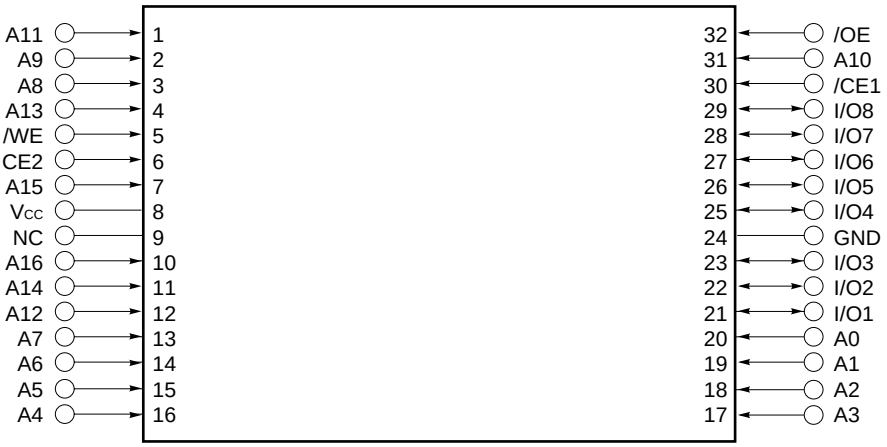
Remark Refer to **Package Drawings** for the 1-pin index mark.

32-pin PLASTIC TSOP(I) (8x20) (Normal bent)

[μPD431000AGZ-xxL-KJH]

[μPD431000AGZ-xxLL-KJH]

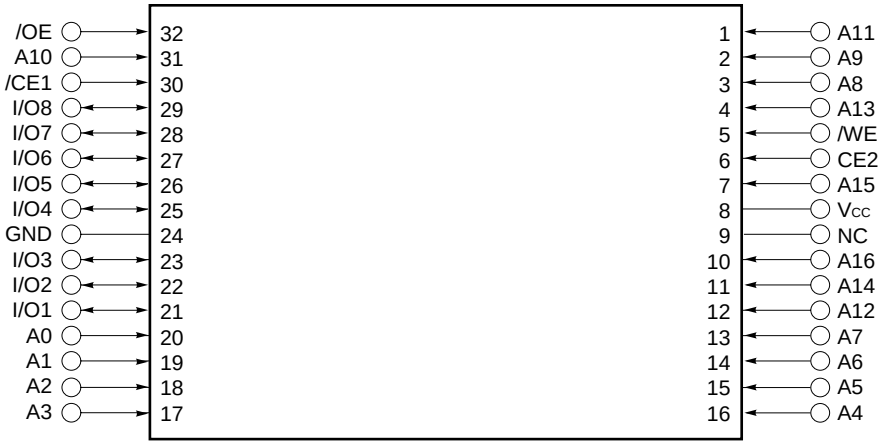
[μPD431000AGZ-Bxx-KJH]



32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)

[μPD431000AGZ-xxLL-KKH]

[μPD431000AGZ-Bxx-KKH]



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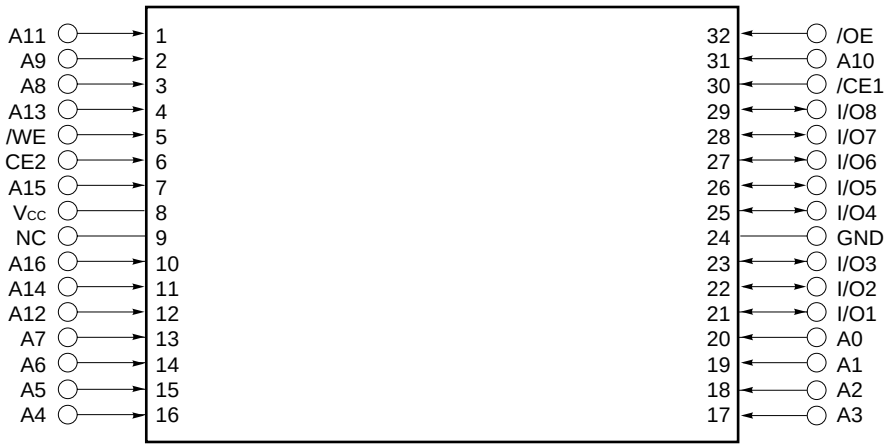
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

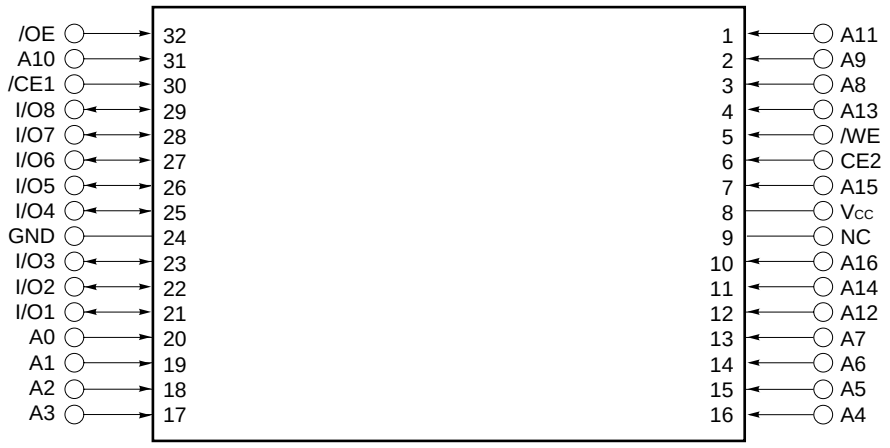
32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent)

[μPD431000AGU-Bxx-9JH]



★ **32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)**

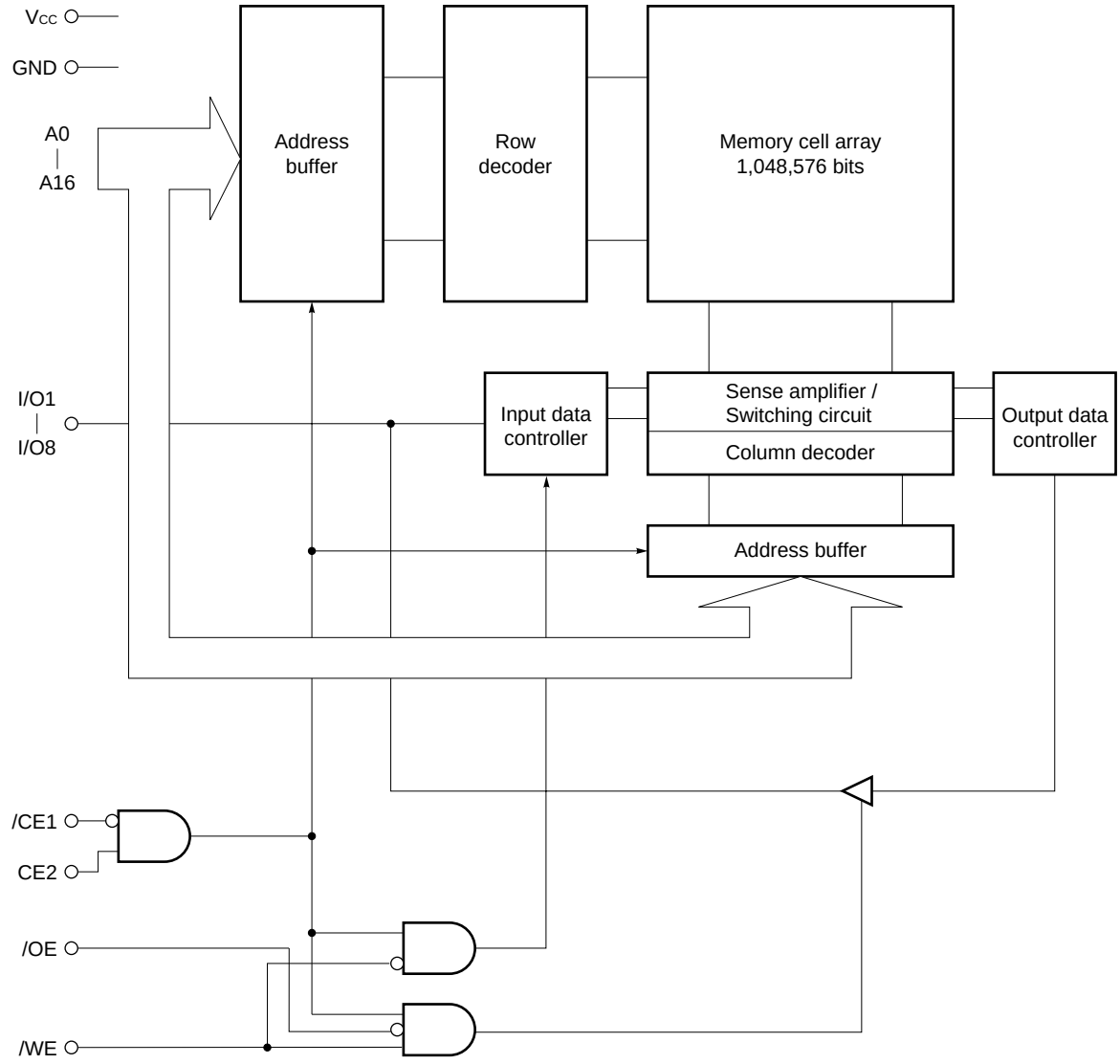
[μPD431000AGU-Bxx-9KH]



A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
H	×	×	×	Not selected	High impedance	I_{SB}
×	L	×	×			
L	H	H	H	Output disable		I_{CCA}
L	H	L	H	Read	D_{OUT}	
L	H	×	L	Write	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +7.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC} + 0.5	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD431000A-xxL μPD431000A-xxLL		μPD431000A-Axx		μPD431000A-Bxx		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	V_{IH}		2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	2.2	V_{CC}+0.5	V
Low level input voltage	V_{IL}		–0.3 Note	+0.8	–0.3 Note	+0.5	–0.3 Note	+0.5	V
Operating ambient temperature	T_A		0	70	0	70	0	70	°C

Note –3.0 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			6	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Parameter	Symbol	Test condition	μPD431000A-xxL			μPD431000A-xxLL			μPD431000A-Axx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	–1.0		+1.0	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA		40	70		40	70		40	70	mA
		Minimum cycle time $V_{CC} \leq 3.6$ V			–			–			35	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA,			15			15			15	
		Cycle time = ∞ $V_{CC} \leq 3.6$ V			–			–			8	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, $V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V			10			10			10	
		$V_{CC} \leq 3.6$ V			–			–			8	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}			3			3			3	mA
		$V_{CC} \leq 3.6$ V			–			–			2	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V,		2	100		1	20		1	20	μA
		CE2 ≥ V_{CC} – 0.2 V $V_{CC} \leq 3.6$ V			–			–		0.5	13	
	I_{SB2}	CE2 ≤ 0.2 V		2	100		1	20		1	20	
		$V_{CC} \leq 3.6$ V		–	–		–	–		0.5	13	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, $V_{CC} \geq 4.5$ V	2.4			2.4			2.4			V
		I_{OH} = –0.5 mA	–			–			2.4			
	V_{OH2}	I_{OH} = –0.02 mA	–			–			V_{CC}–0.1			
Low level output voltage	V_{OL1}	I_{OL} = 2.1 mA, $V_{CC} \geq 4.5$ V			0.4			0.4			0.4	V
		I_{OL} = 1.0 mA			–			–			0.4	
	V_{OL2}	I_{OL} = 0.02 mA			–			–			0.1	

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These DC characteristics are in common regardless product classification.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Parameter	Symbol	Test condition		μPD431000A-Bxx			Unit
				MIN.	TYP.	MAX.	
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}		–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CE1 = V_{IH} or CE2 = V_{IL} or /WE = V_{IL} or /OE = V_{IH}		–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA			40	70	mA
		Minimum cycle time	$V_{CC} \leq$ 3.3 V			30	
	I_{CCA2}	/CE1 = V_{IL}, CE2 = V_{IH}, $I_{I/O}$ = 0 mA,				15	
		Cycle time = ∞	$V_{CC} \leq$ 3.3 V			7	
	I_{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA,				10	
		$V_{IL} \leq$ 0.2 V, $V_{IH} \geq V_{CC}$ – 0.2 V	$V_{CC} \leq$ 3.3 V			7	
Standby supply current	I_{SB}	/CE1 = V_{IH} or CE2 = V_{IL}				3	mA
			$V_{CC} \leq$ 3.3 V			2	
	I_{SB1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V			1	20	μA
			$V_{CC} \leq$ 3.3 V		0.5	11	
	I_{SB2}	CE2 ≤ 0.2 V			1	20	
			$V_{CC} \leq$ 3.3 V		0.5	11	
High level output voltage	V_{OH1}	I_{OH} = –1.0 mA, $V_{CC} \geq$ 4.5 V		2.4			V
		I_{OH} = –0.5 mA		2.4			
	V_{OH2}	I_{OH} = –0.02 mA		V_{CC}–0.1			
Low level output voltage	V_{OL1}	I_{OL} = 2.1 mA, $V_{CC} \geq$ 4.5 V				0.4	V
		I_{OL} = 1.0 mA				0.4	
	V_{OL2}	I_{OL} = 0.02 mA				0.1	

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

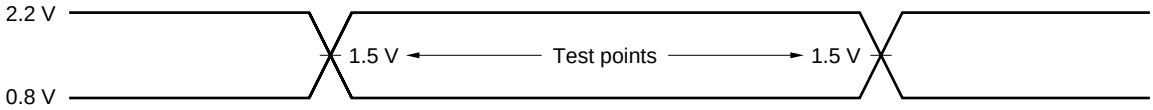
2. These DC characteristics are in common regardless product classification.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

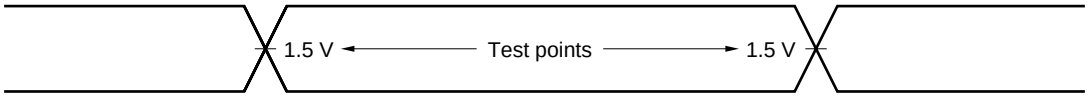
AC Test Conditions

[μPD431000A-70L, μPD431000A-85L, μPD431000A-70LL, μPD431000A-85LL]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

Figure 1

(t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH})

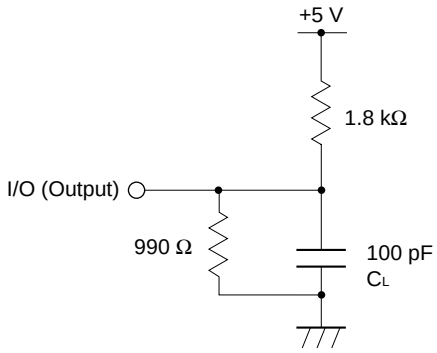
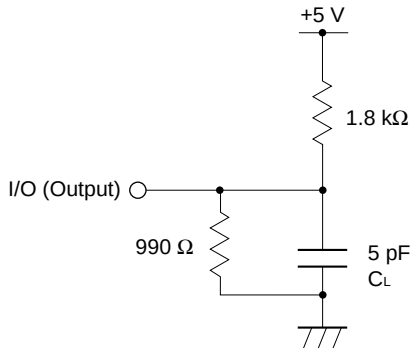


Figure 2

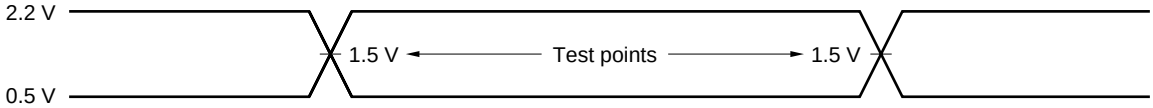
(t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{OW})



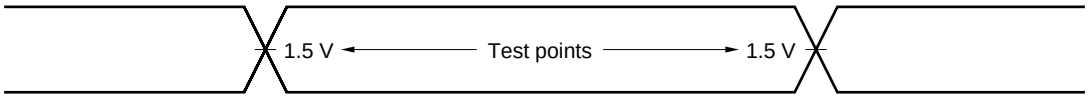
Remark C_L includes capacitance of the probe and jig, and stray capacitance.

★ **[μPD431000A-A10, μPD431000A-B10, μPD431000A-B12, μPD431000A-B15]**

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

AC characteristics should be measured with the following output load conditions.

Part number	Output load condition	
	t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH}	t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{OW}
★ μPD431000A-A10, μPD431000A-B10, μPD431000A-B12	1TTL + 50 pF	1TTL + 5 pF
μPD431000A-B15	1TTL + 100 pF	1TTL + 5 pF

Read Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				$V_{CC} \geq 3.0$ V		Unit	Condition
		μPD431000A-70 μPD431000A-Axx μPD431000A-Bxx		μPD431000A-85		μPD431000A-A10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	**Note**
/CE1 access time	t_{CO1}		70		85		100	ns	
CE2 access time	t_{CO2}		70		85		100	ns	
/OE to output valid	t_{OE}		35		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		25		30		35	ns	
CE2 to output in high impedance	t_{HZ2}		25		30		35	ns	
/OE to output in high impedance	t_{OHZ}		25		30		35	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

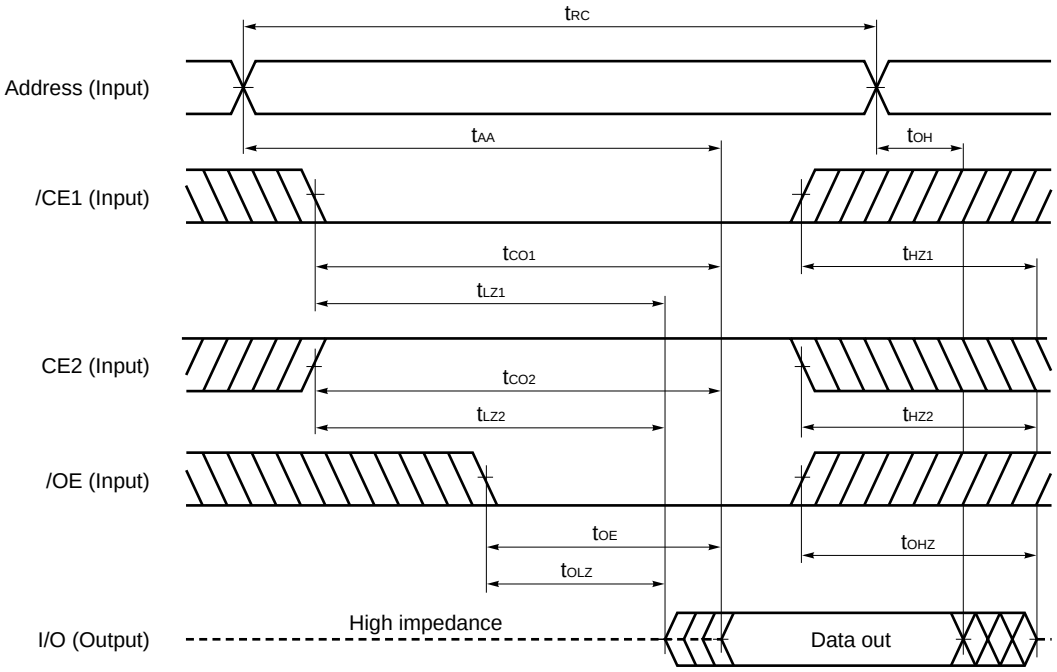
★ **Read Cycle (2/2)**

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		150		ns	
Address access time	t_{AA}		100		120		150	ns	**Note**
/CE1 access time	t_{CO1}		100		120		150	ns	
CE2 access time	t_{CO2}		100		120		150	ns	
/OE to output valid	t_{OE}		50		60		70	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
/CE1 to output in low impedance	t_{LZ1}	10		10		10		ns	
CE2 to output in low impedance	t_{LZ2}	10		10		10		ns	
/OE to output in low impedance	t_{OLZ}	5		5		5		ns	
/CE1 to output in high impedance	t_{HZ1}		35		40		50	ns	
CE2 to output in high impedance	t_{HZ2}		35		40		50	ns	
/OE to output in high impedance	t_{OHZ}		35		40		50	ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/2)

Parameter	Symbol	$V_{CC} \geq 4.5$ V				$V_{CC} \geq 3.0$ V		Unit	Condition
		μPD431000A-70 μPD431000A-Axx μPD431000A-Bxx		μPD431000A-85		μPD431000A-A10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		85		100		ns	
/CE1 to end of write	t_{CW1}	55		70		80		ns	
CE2 to end of write	t_{CW2}	55		70		80		ns	
Address valid to end of write	t_{AW}	55		70		80		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		60		60		ns	
Write recovery time	t_{WR}	5		5		0		ns	
Data valid to end of write	t_{DW}	35		35		60		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		25		30		35	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless package types.

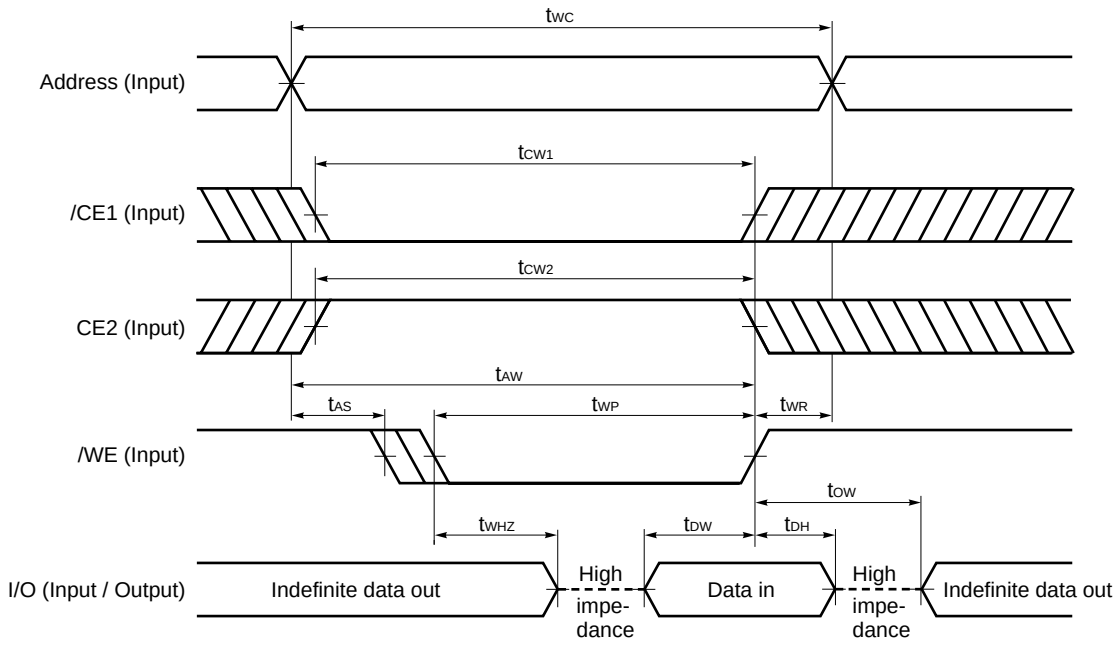
★ **Write Cycle (2/2)**

Parameter	Symbol	$V_{CC} \geq 2.7$ V						Unit	Condition
		μPD431000A-B10		μPD431000A-B12		μPD431000A-B15			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		150		ns	
/CE1 to end of write	t_{CW1}	80		100		120		ns	
CE2 to end of write	t_{CW2}	80		100		120		ns	
Address valid to end of write	t_{AW}	80		100		120		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	60		85		100		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	60		60		80		ns	
Data hold time	t_{DH}	0		0		0		ns	
/WE to output in high impedance	t_{WHZ}		35		40		50	ns	**Note**
Output active from end of write	t_{OW}	5		5		5		ns	

Note See the **output load**.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

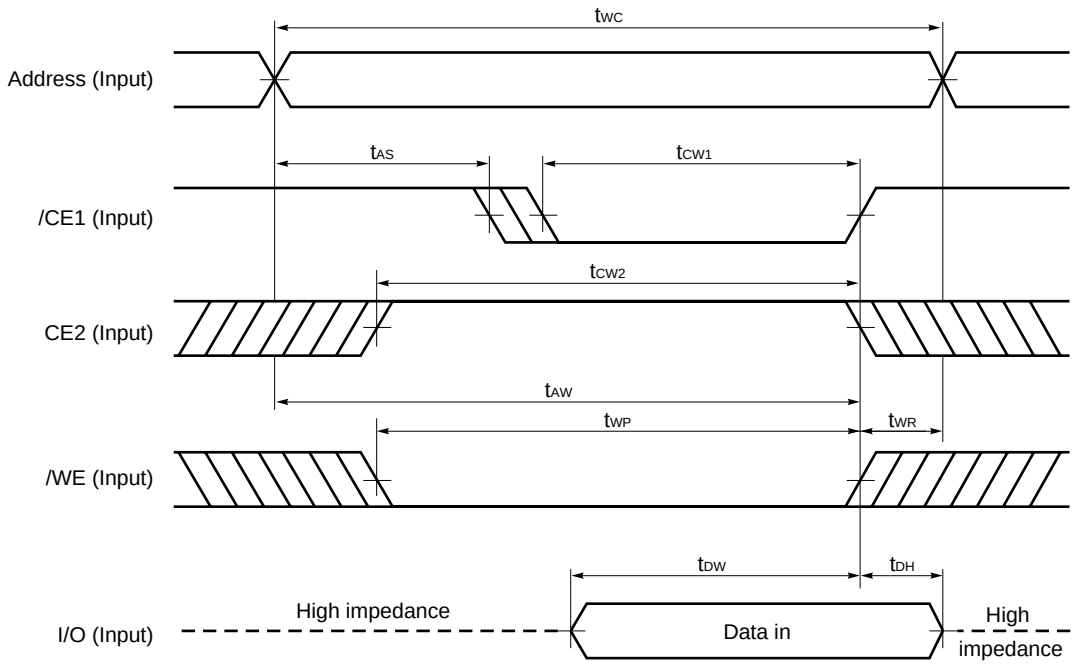
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CE1 Controlled)

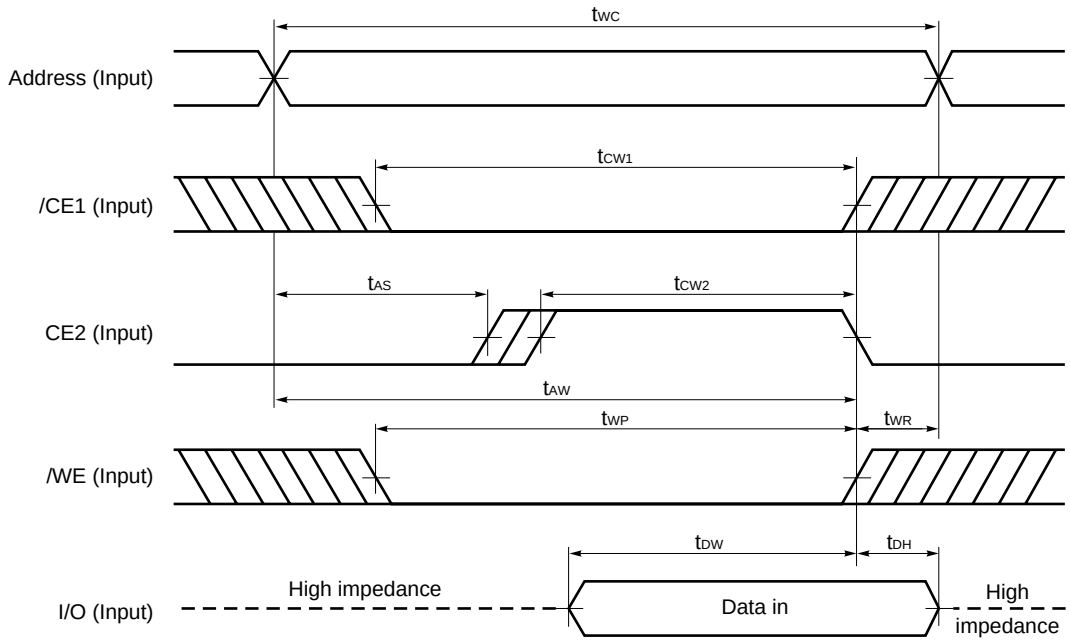


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Low V_{CC} Data Retention Characteristics (T_A = 0 to 70 °C)

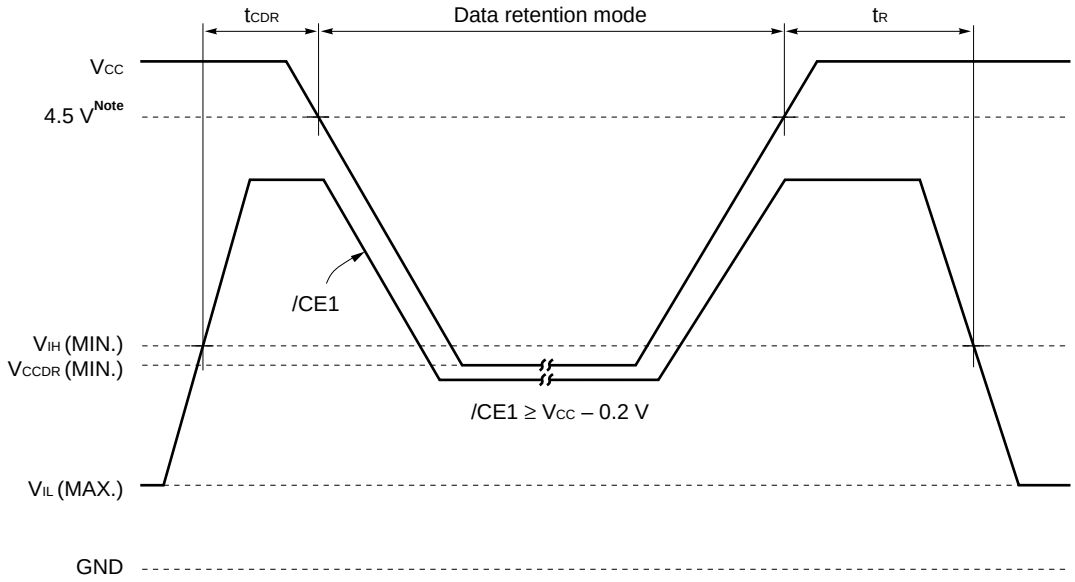
Parameter	Symbol	Test Condition	μPD431000A-xxL			μPD431000A-xxLL μPD431000A-Axx μPD431000A-Bxx			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V_{CCDR1}	/CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V	2.0		5.5	2.0		5.5	V
	V_{CCDR2}	CE2 ≤ 0.2 V	2.0		5.5	2.0		5.5	
Data retention supply current	I_{CCDR1}	V_{CC} = 3.0 V, /CE1 ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V		1	50 Note1		0.5	10 Note2	μA
	I_{CCDR2}	V_{CC} = 3.0 V, CE2 ≤ 0.2 V		1	50 Note1		0.5	10 Note2	
Chip deselection to data retention mode	t_{CDR}		0			0			ns
Operation recovery time	t_R		5			5			ms

Notes 1. 15 μA (T_A ≤ 40 °C)

2. 3 μA (T_A ≤ 40 °C)

Data Retention Timing Chart

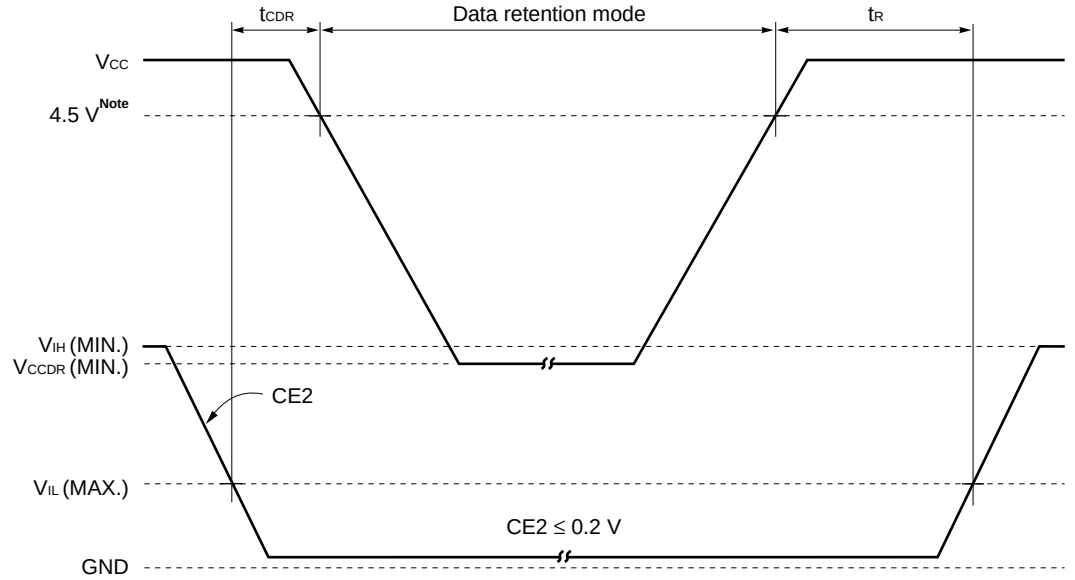
(1) /CE1 Controlled



Note A version : 3.0 V, B version : 2.7 V

Remark On the data retention mode by controlling /CE1, the input level of CE2 must be CE2 ≥ V_{CC} – 0.2 V or CE2 ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

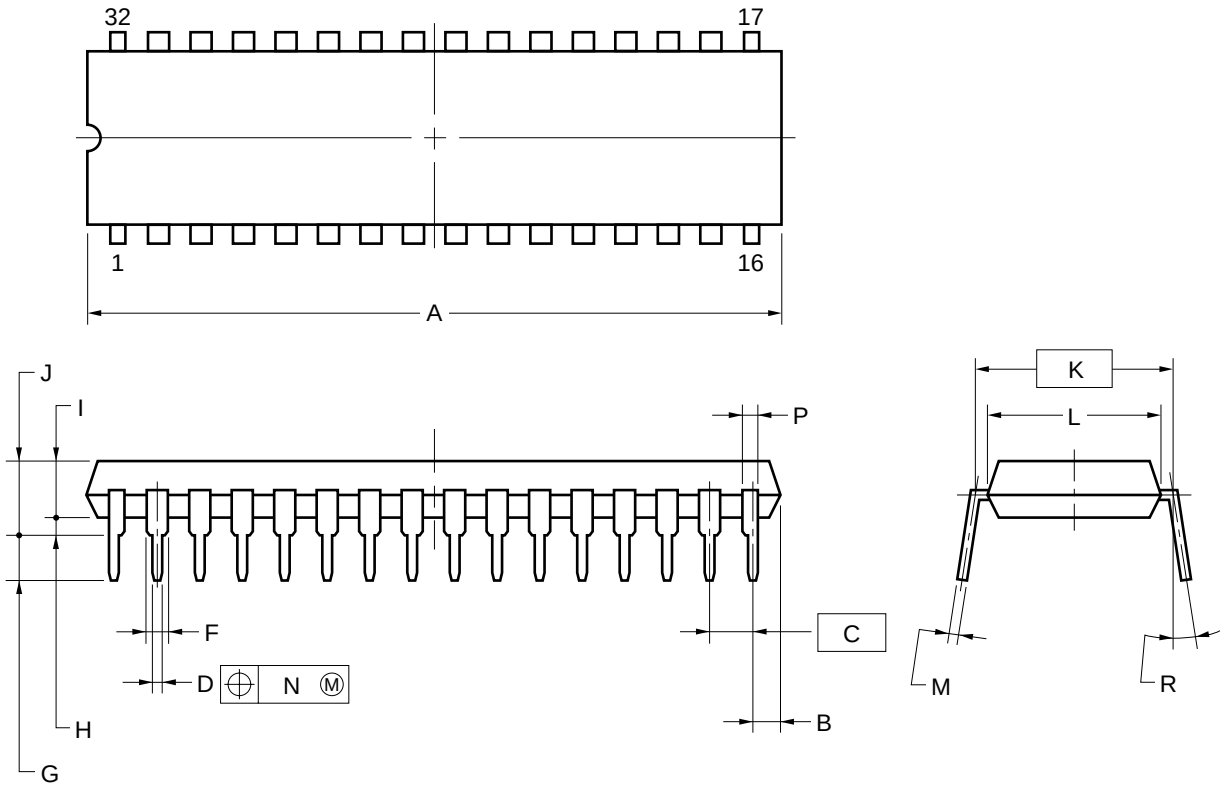


Note A version : 3.0 V, B version : 2.7 V

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32-PIN PLASTIC DIP (15.24mm(600))



NOTES

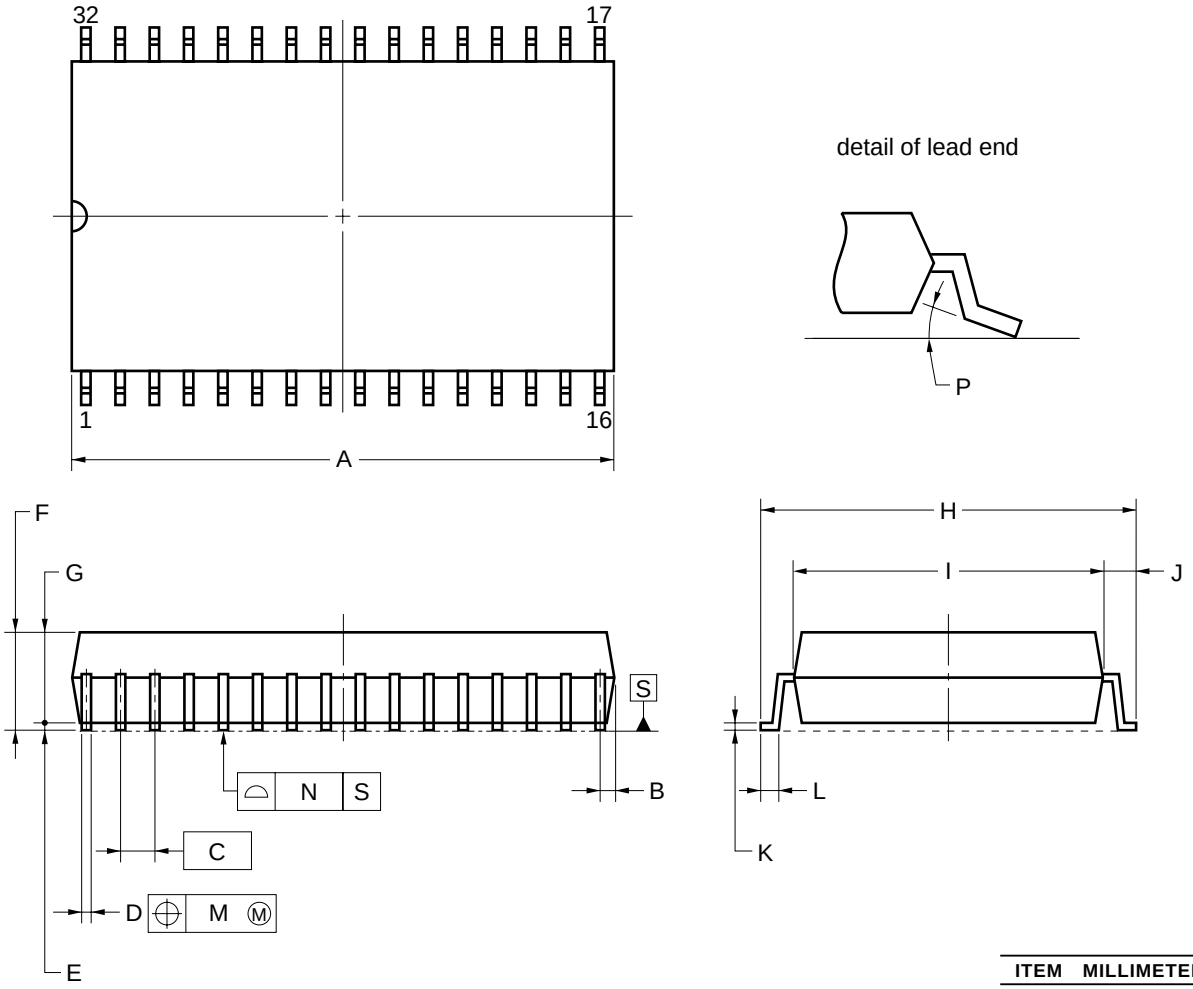
1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	40.64 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.1 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	15.24 (T.P.)
L	13.2
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	0.9 MIN.
R	0 - 15°

P32C-100-600A-2

32-PIN PLASTIC SOP (13.34 mm (525))



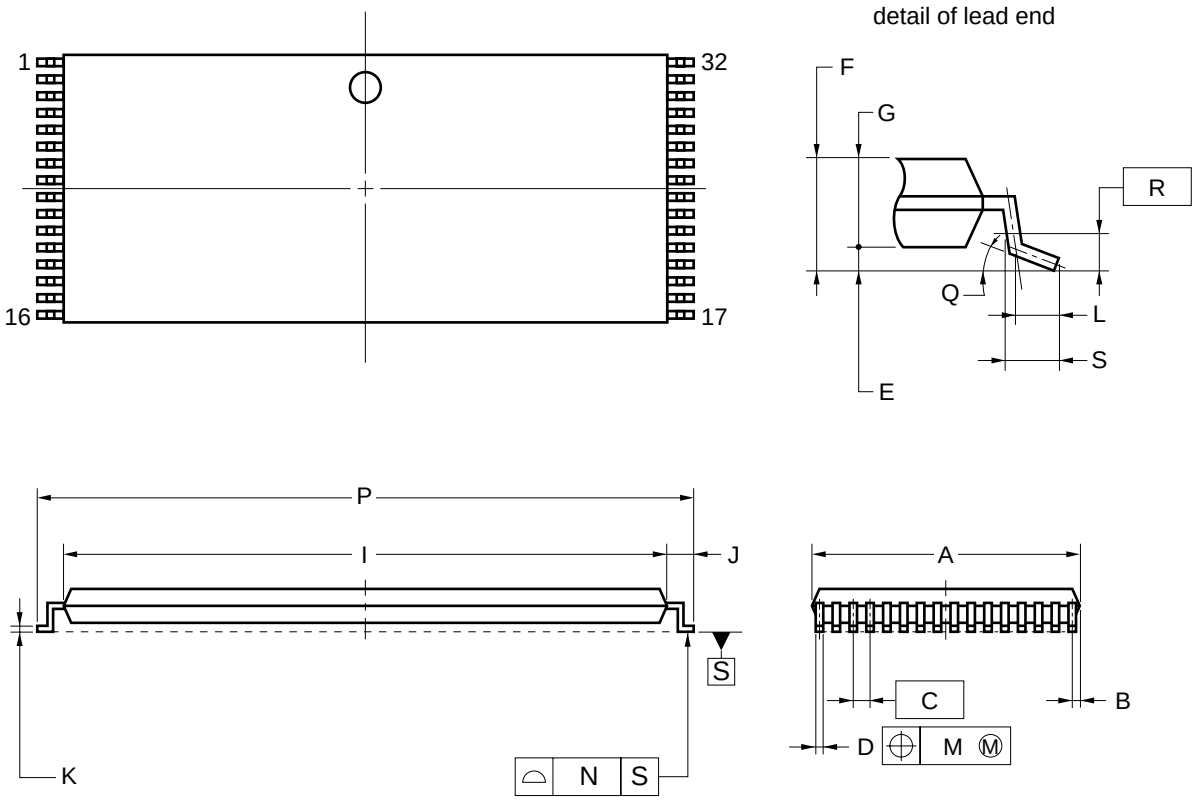
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	20.61 MAX.
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.40^{+0.10}_{-0.05}$
E	0.15±0.05
F	2.95 MAX.
G	2.7
H	14.1±0.3
I	11.3
J	1.4±0.2
K	$0.20^{+0.10}_{-0.05}$
L	0.8±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P32GW-50-525A-1

32-PIN PLASTIC TSOP(I) (8x20)



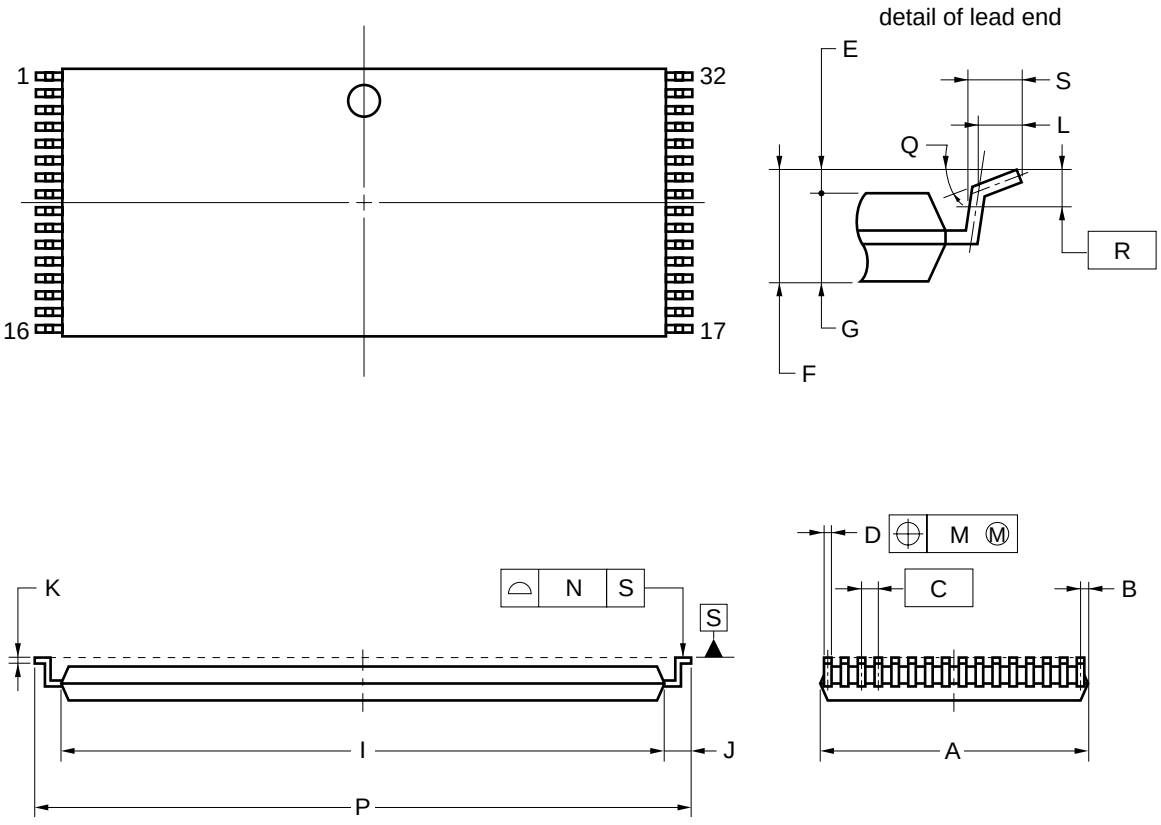
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S32GZ-50-KJH1-2

32-PIN PLASTIC TSOP(I) (8x20)



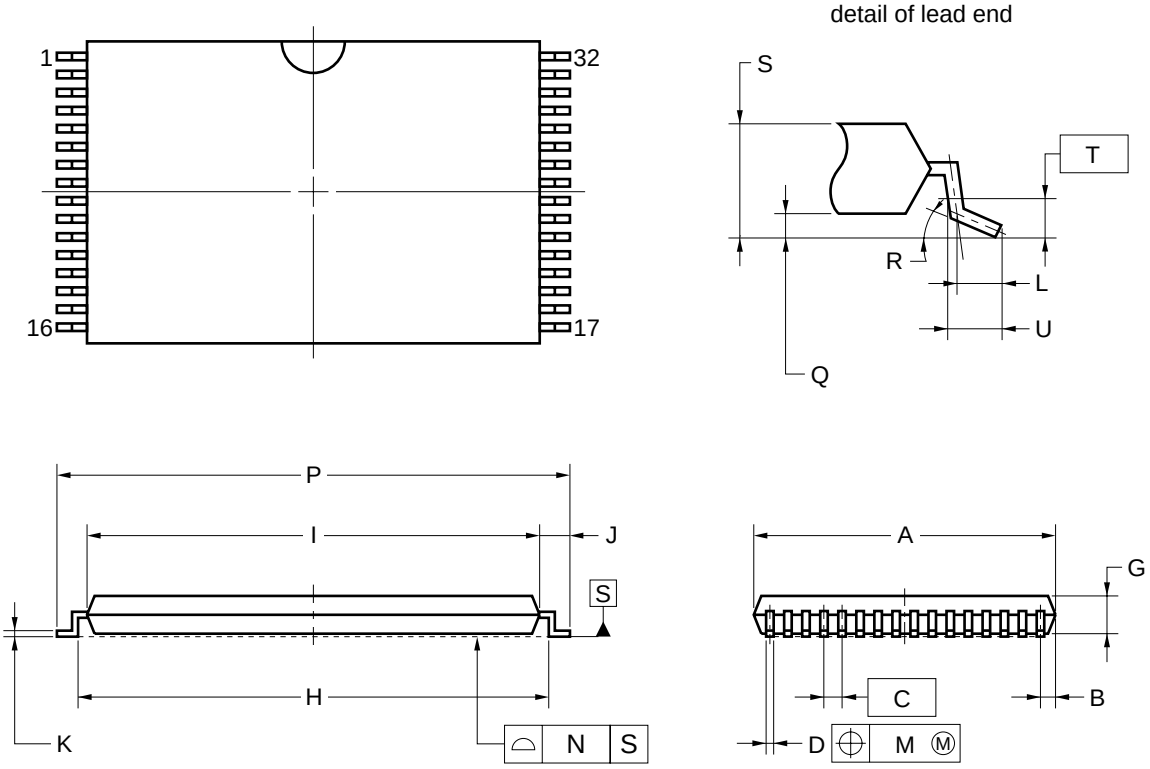
NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	0.97±0.08
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S32GZ-50-KKH1-2

32-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

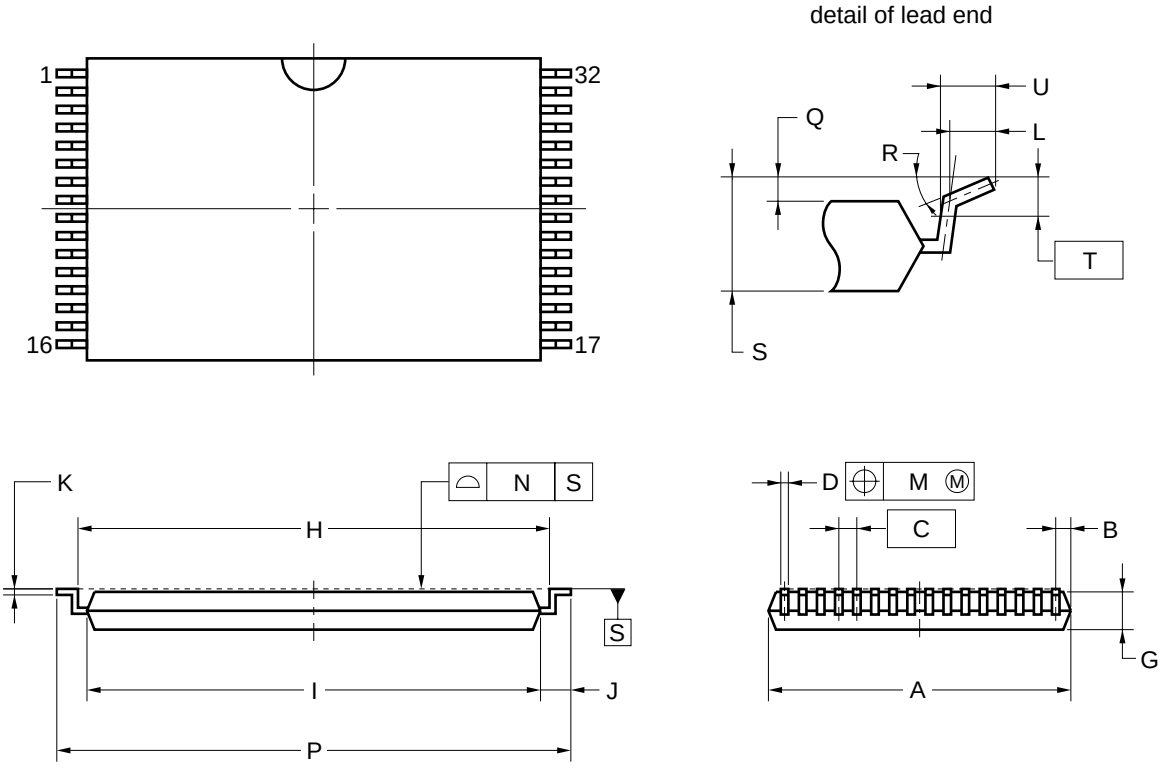
1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9JH-2

★ 32-PIN PLASTIC TSOP(I) (8x13.4)



NOTES

1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS
A	8.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
G	1.0±0.05
H	12.4±0.2
I	11.8±0.1
J	0.8±0.2
K	$0.145^{+0.025}_{-0.015}$
L	0.5
M	0.08
N	0.08
P	13.4±0.2
Q	0.1±0.05
R	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
S	1.2 MAX.
T	0.25
U	0.6±0.15

P32GU-50-9KH-2

Recommended Soldering Conditions

The following conditions must be met when soldering conditions of the μPD431000A.

For more details, refer to our document **"SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).**

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD431000AGW-xxL : 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-xxLL : 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Axx : 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Bxx : 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGZ-xxL-KJH : 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGZ-xxLL-KJH : 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGZ-xxLL-KKH : 32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)
μPD431000AGZ-Bxx-KJH : 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGZ-Bxx-KKH : 32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)
μPD431000AGU-Bxx-9JH : 32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent)
★ μPD431000AGU-Bxx-9KH : 32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)

Please consult with our sales offices.

Types of Through Hole Mount Device

μPD431000ACZ-xxL: 32-pin PLASTIC DIP (15.24 mm (600))
μPD431000ACZ-xxLL: 32-pin PLASTIC DIP (15.24 mm (600))

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature : 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition -> This edition)
	This edition	Previous edition			
11th edition/ April 2002	Throughout	Throughout	Addition	Part number	μPD431000AGZ-B10-KJH μPD431000AGU-B10-9JH μPD431000AGU-B10-9KH
	p. 2, 6, 25, 26	p. 2, 6, 25	Addition	Package	32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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