National Semiconductor

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MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting CMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting CMOS Buffer

General Description

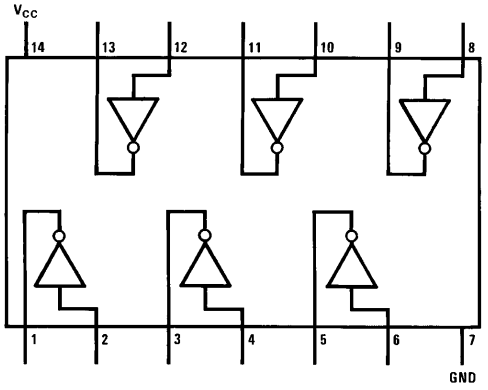
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Fan out of 2 driving standard TTL

Connection Diagrams

Dual-In-Line Package
MM54C901/MM74C901
MM54C903/MM74C903

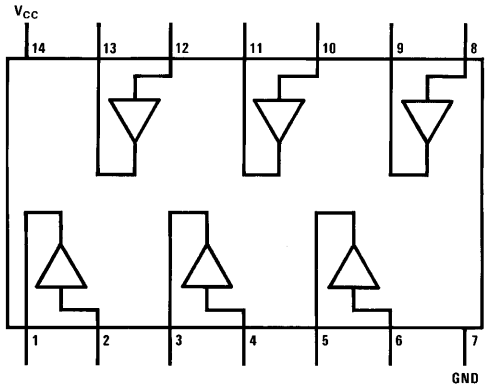


TL/F/5909–1

Top View

Order Number MM54C901, MM74C901, MM54C903 or MM74C903

Dual-In-Line Package
MM54C902/MM74C902
MM54C904/MM74C904



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Top View
Order Number MM54C902, MM74C902, MM54C904 or MM74C904

MM54C901/MM74C901 (TTL), MM54C903/MM74C903 (CMOS) Hex Inverting Buffer
MM54C902/MM74C902 (TTL), MM54C904/MM74C904 (CMOS) Hex Non-Inverting Buffer

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Input Pin	
MM54C901/MM74C901	$-0.3V$ to $+15V$
MM54C902/MM74C902	$-0.3V$ to $+15V$
MM54C903/MM74C903	$V_{CC} - 17V$ to $V_{CC} + 0.3V$
MM54C904/MM74C904	$V_{CC} - 17V$ to $V_{CC} + 0.3V$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating Temperature Range (T_A)	
MM54C901, MM54C902, MM54C903, MM54C904	$-55°C$ to $+125°C$
MM74C901, MM74C902, MM74C903, MM74C904	$-40°C$ to $+85°C$
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	15	μA
TTL TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
CMOS TO TTL						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$	4.0			V
	MM54C902, MM54C904	$V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	MM74C901, MM74C903	$V_{CC} = 4.75V$	4.25			V
	MM74C902, MM74C904	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$			1.0	V
	MM54C902, MM54C904	$V_{CC} = 4.5V$			1.5	V
	MM74C901, MM74C903	$V_{CC} = 4.75V$			1.0	V
	MM74C902, MM74C904	$V_{CC} = 4.75V$			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -800\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = -800\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$, $I_O = 2.6$ mA			0.4	V
	MM54C902, MM54C904	$V_{CC} = 4.5V$, $I_O = 3.2$ mA			0.4	V
	MM74C901, MM74C903	$V_{CC} = 4.75V$, $I_O = 2.6$ mA			0.4	V
	MM74C902, MM74C904	$V_{CC} = 4.75V$, $I_O = 3.2$ mA			0.4	V

DC Electrical Characteristics (Continued)

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C901/MM74C901, MM54C903/MM74C903)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = 0V$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = 0V$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = V_{CC}$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	3.8			mA
(MM54C902/MM74C902, MM54C904/MM74C904)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = 0V$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$ $T_A = 25°C$, $V_{IN} = 0V$	3.8			mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C901/MM74C901, MM54C903/MM74C903						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		38 22	70 30	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		21 13	35 20	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		14		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF
MM54C902/MM74C902, MM54C904/MM74C904						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		57 27	90 40	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		54 25	90 40	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		50		pF

*AC Parameters are guaranteed by DC correlated testing.

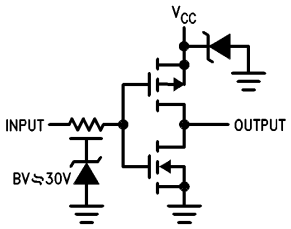
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Logic Diagrams

MM54C901/MM74C901
CMOS to TTL Inverting Buffer



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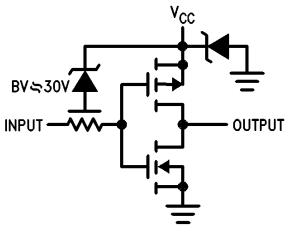
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



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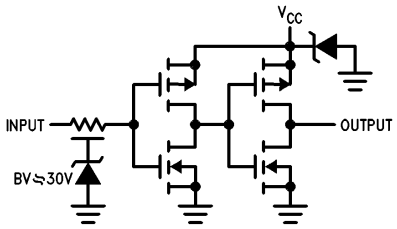
MM54C902/MM74C902
CMOS to TTL Buffer



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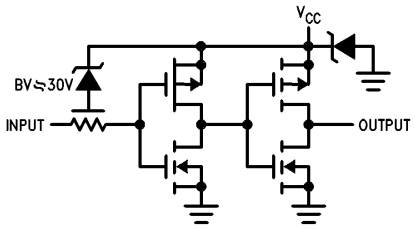
MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



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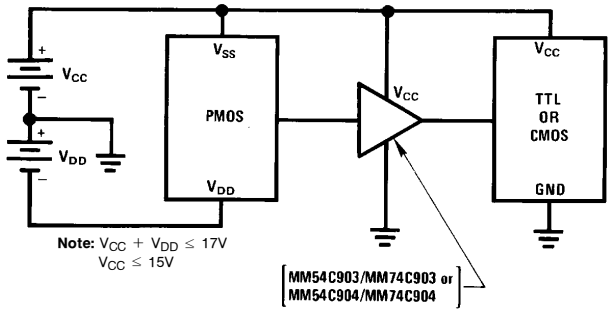
Typical Applications

PMOS to CMOS or TTL Interface



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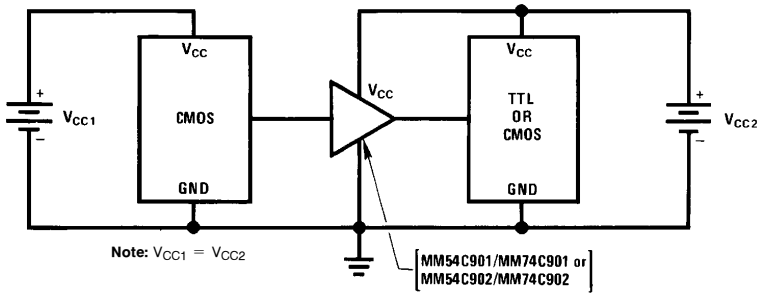
CMOS to TTL or CMOS at a Lower V_{CC}



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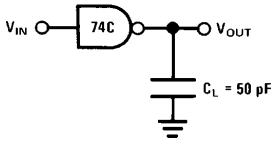
AC Test Circuit and Switching Time Waveforms



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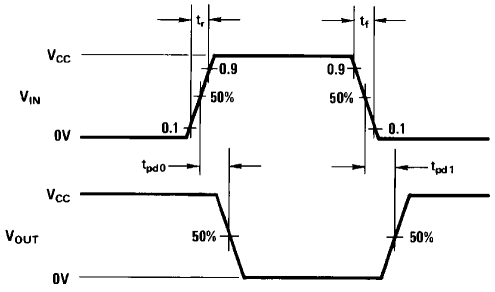
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS



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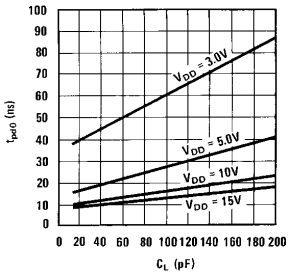
Typical Performance Characteristics

Typical Propagation Delay to a Logical "0" for the MM54C901/MM74C901 and MM54C903/MM74C903



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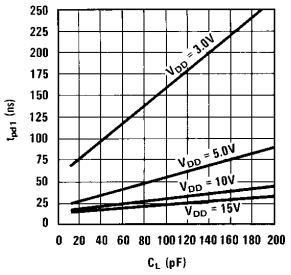
Typical Propagation Delay to a Logical "1" for the MM54C901/MM74C901 and M54C903/MM74C903



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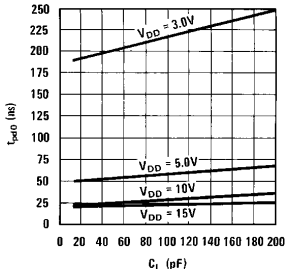
Typical Propagation Delay to a Logical "0" for the MM54C902/MM74C902 and MM54C904/MM74C904



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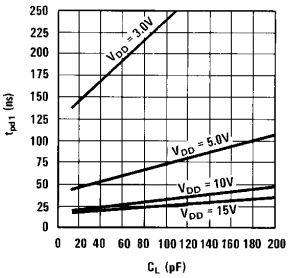
Typical Propagation Delay to a Logical "1" for the MM54C902/MM74C902 and MM54C904/MM74C904



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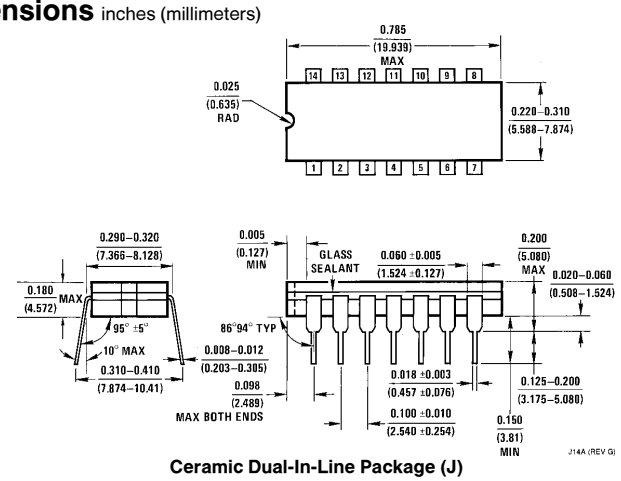
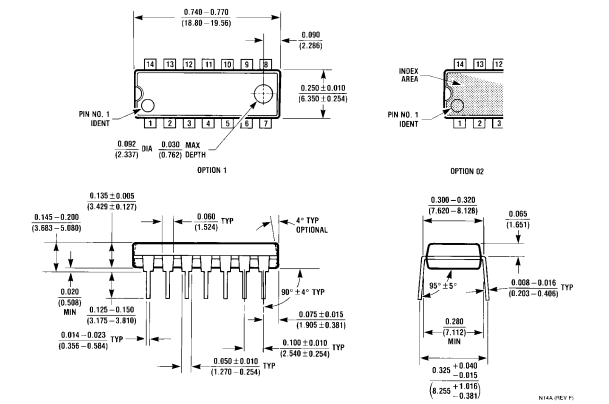
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number MM54C901J, MM74C901J, MM54C902J, MM74C902J, MM54C903J, MM74C903J, MM54C904J or MM74C904J
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number MM54C901N, MM74C901N, MM54C902N, MM74C902N, MM54C903N, MM74C903N, MM54C904N or MM74C904N
NS Package Number N14A

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