CMOS 12-Bit, 6 Word, FIFO, DAC

AD7544

PRELIMINARY TECHNICAL DATA

FEATURES

- ±1/2LSB Nonlinearity from T_{min} to T_{max}
- Monotonicity Guaranteed for 11- and 12-Bit Versions
- Twelve-Bit Wide, Six-Word Deep First-In First-Out (FIFO) Buffer Memory
- FIFO Status Flags for Input/Output Handshaking
- Directly Interfaces with 16-Bit Microprocessors
- Low Gain Drift, Typically 2ppm/°C
- ±1LSB max Gain Error
- Latch-Up Proof
- Single +5V Supply

GENERAL DESCRIPTION

The AD7544 is a 12-bit monolithic CMOS DAC with a 12-bit wide, 6-word deep, First-In First-Out (FIFO) Register stack. Twelve-bit words are written to the top of the stack under the control of $\overline{WR}$ (Write) and WREN (Write Enable). The 12-bit word then falls through the stack into the last empty register nearest the bottom of the stack. Hence, the stack is full after six write instructions. There are two status flags associated with the stack, SFUL (Stack Full) and SAMT (Stack Almost Empty, one word remaining).

The contents of the stack can be rolled down towards the DAC register under control of $\overline{RL}$ (Roll) and $\overline{RLEN}$ (Roll ENable). The DAC register, under control of LDAC (Load DAC), may be loaded with either word 1 or word 2 of the stack depending upon the word-selector control input W1/$\overline{W2}$. System Reset $\overline{RST}$ loads all 0s into the DAC register and resets the stack register control flip-flops to allow a full six-word load operation.

ORDERING INFORMATION

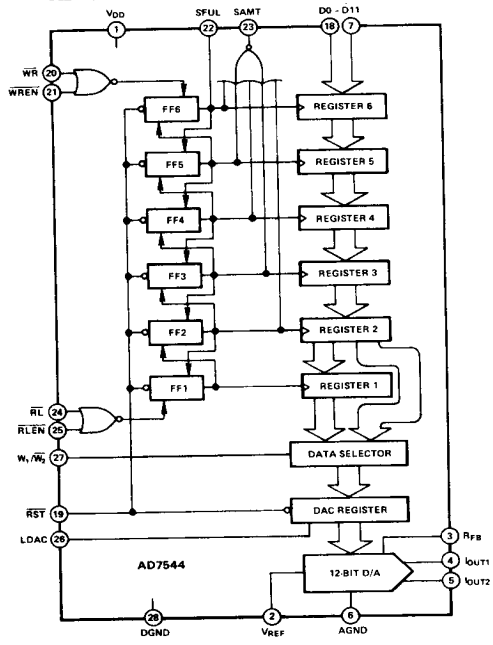
Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Temperature Range 0 to +70°C	-25°C to +85°C	-55°C to +125°C
±1LSB	±12.3LSBs	AD7544JN	AD7544AD	AD7544SD
±1/2LSB	±12.3LSBs	AD7544KN	AD7544BD	AD7544TD
±1/2LSB	±1LSB	AD7544GKN	AD7544GBD	AD7544GTD

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D28B)
Suffix N: Plastic DIP – (N28A)

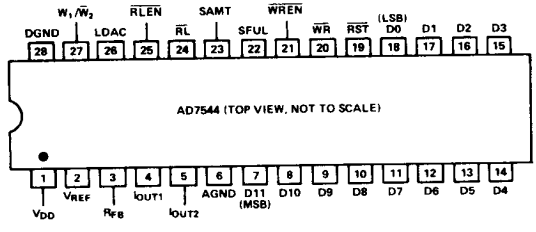
[1] See Section 20 for outline information.

AD7544 FUNCTIONAL BLOCK DIAGRAM



28-PIN DIP

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = 5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GKN, GBD, GTD	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 4 & 5)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.002	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Propagation Delay[2]	185	230	250	ns max	I_{OUT1} load = 100Ω, C_{EXT} = 13pF. Measured from LDAC (Pin 26) going high to 90% of final output current for a full-scale change.
Stack Propagation Delay	1.26	1.4	1.6	μs max	I_{OUT1} load = 100Ω, C_{EXT} = 13pF. LDAC held HIGH. Measured from $\overline{WR}$ (Pin 20) going high to 90% of final output current for a full-scale data input change.
Digitial Charge Injection[2]	700	700	700	nVsecs typ	Typical value included for design guidance only
Multiplying Feedthrough Error[2]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz Sine Wave
REFERENCE INPUT					
Input Resistance (Pin 2)	7/12/20	7/12/20	7/12/20	kΩ min/typ/max	
Input Resistance Temperature Coefficient	-300	-300	-300	ppm/°C typ	
ANALOG OUTPUTS					
Output Capacitance[3]					
C_{OUT1}	75	75	75	pF max	DAC Register loaded with all 0s
C_{OUT2}	260	260	260	pF max	
C_{OUT1}	260	260	260	pF max	DAC Register loaded with all 1s
C_{OUT2}	75	75	75	pF max	
DIGITAL INPUTS					
V_{IH} (Input High Voltage)	3.0	3.0	3.0	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	V max	
I_{IN}, Input Current[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
CIN, Input Capacitance[3]	8	8	8	pF max	
Input Coding	Binary or Offset Binary				See Tables 5 & 6
DIGITAL OUTPUTS					
V_{OH} (Output High Voltage)	+4.0	+4.0	+4.0	V min	I_{SOURCE} = -40μA
V_{OL} (Output Low Voltage)	+0.6	+0.8	+0.8	V max	I_{SINK} = 1.6mA
SWITCHING CHARACTERISTICS[5]					
t_{WR}	75	75	95	ns min	Write Pulse Width
t_{WRS}	0	0	0	ns min	Write Enable Setup Time
t_{WRH}	0	0	0	ns min	Write Enable Hold Time
t_{WDS}	220	290	330	ns max	Write to Data Setup Time
t_{WDH}	270	320	375	ns min	Write to Data Hold Time
t_{WMT}	400	500	600	ns max	Stack Almost Empty Flag LOW Response Time
t_{WFL}	320	420	450	ns max	Stack Full Flag HIGH Response Time
t_{RL}	75	75	95	ns min	Roll Pulse Width
t_{RLS}	0	0	0	ns min	Roll Enable Setup Time
t_{RLH}	0	0	0	ns min	Roll Enable Hold Time
t_{RFL}	1.1	1.3	1.44	μs max	Stack Full Flag LOW Response Time
t_{RMT}	380	500	580	ns max	Stack Almost Empty Flag HIGH Response Time
t_{LDAC}	120	160	180	ns min	Load DAC Pulse Width
t_{WSS}	135	165	230	ns min	Word Select Setup Time
t_{WSH}	0	0	0	ns min	Word Select Hold Time
$t_{\overline{RST}}$	75	100	140	ns min	Reset Pulse Width
POWER SUPPLY					
V_{DD}	+5	+5	+5	V	
I_{DD}	2	2	2	mA max	Digital Inputs = V_{IH} or V_{IL}
	100	500	500	μA max	Digital Inputs = 0V or V_{DD}

NOTES

[1] Temperature range as follows: JN, KN, LN, GKN Versions: 0 to +70°C
AD, BD, CD, GBD Versions: -25°C to +85°C
SD, TD, UD, GTD Versions: -55°C to +125°C

[2] See definition on next page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current at +25°C is 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . 0V, +7V
V_{DD} to AGND . . . . . 0V, +7V
AGND to DGND . . . . . $\pm V_{DD}$
DGND to AGND . . . . . $\pm V_{DD}$
Digital Input Voltage to DGND
(pins 7 - 21, 24 - 27) . . . . . -0.3V, +15V
Digital Output Voltage to DGND
(pins 22, 23) . . . . . -0.3V, +15V
V_{PIN4}, V_{PIN5} to AGND . . . . . -0.3V, +15V
V_{REF} to AGND . . . . . ±25V
V_{RFB} to AGND . . . . . ±25V

Operating Temperature Range
JN, KN, GKN Versions . . . . . 0 to +70°C
AD, BD, GBD Versions . . . . . -25°C to +85°C
SD, TD, GTD Versions . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
Power Dissipation (Package)
Plastic (Suffix N)
to +50°C 1200mW
Derate Above +50°C by . . . . . 12mW/°C
Ceramic (Suffix D)
to +50°C 1000mW
Derate Above +50°C by . . . . . 10mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed as a percentage of full-scale range.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7544, ideal full-scale output is V_{REF} - 1LSB. Gain error is adjustable to zero.

DIGITIAL CHARGE INJECTION
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA secs or nV secs depending upon whether the glitch is measured as a current or voltage signal. Digitial charge injection is measured with the reference input of the DAC connected to ground.

PROPAGATION DELAY
This is a measure of the internal delays of the circuit and is defined as the time from LDAC going high to the analog output current reaching 90% of its final value for a full-scale change.

FSR
This is an abbreviation for Full Scale Range. For a 12-bit converter with a reference input of 10V the FSR is 10 X (4095/4096) Volts.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with DAC Register loaded to all 0s or at OUT2 with DAC Register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

Pin No.	Name	Function	Pin No.	Name	Function
1	V_{DD}	+5V Supply	18	D0	Data Input (LSB)
2	V_{REF}	±20V Reference Voltage	19	$\overline{RST}$	Reset, when low resets DAC Register and stack control flip-flops to zero.
3	R_{FB}	DAC Feedback Resistor	20	$\overline{WR}$	Write, with $\overline{WREN}$ low, the trailing edge of $\overline{WR}$ loads data into the lowest available empty register of the stack.
4	I_{OUT1}	Output from R-2R Ladder	21	$\overline{WREN}$	Write Enable.
5	I_{OUT2}	Output from R-2R Ladder	22	SFUL	Stack Full Flag. When HIGH, indicates stack is full. When LOW, indicates less than six words remain in stack.
6	AGND	Analog Ground	23	SAMT	Stack Almost Empty Flag. When HIGH, indicates one word or less remains in the stack. When LOW, indicates more than one word contained in the stack.
7	D11	Data Input (MSB)	24	$\overline{RL}$	Roll, with $\overline{RLEN}$ low the trailing edge of $\overline{RL}$ rolls information down the FIFO stack past the register data-selector.
8	D10	Data Input	25	$\overline{RLEN}$	Roll Enable.
9	D9	Data Input	26	LDAC	Load DAC. Loads information from one of two stack registers into the DAC register (see $W_1/\overline{W_2}$).
10	D8	Data Input	27	$W_1/\overline{W_2}$	WORD1/$\overline{WORD2}$. A HIGH enables WORD 1 through the data-selector, a LOW enables WORD 2.
11	D7	Data Input	28	DGND	Digital Ground.
12	D6	Data Input			
13	D5	Data Input			
14	D4	Data Input			
15	D3	Data Input			
16	D2	Data Input			
17	D1	Data Input			

Table 1. Pin Function Description

AD7544 OPERATION

The AD7544 FIFO stack consists of six 12-bit Data Registers as shown in the Functional Block Diagram. Internally a Stack Register is considered to be empty if the output from its control flip-flop, FFN (Figure 1), is LOW. After a Reset Signal $\overline{RST}$ all control flip-flops are reset LOW and the DAC Register is loaded with all 0s.

Twelve-bit data is written into the stack by exercising $\overline{WR}$ and $\overline{WREN}$. Initially, this data is latched into the top Register of the stack (Register 6) and the output of the FF6 control flip-flop momentarily goes HIGH. If at this instant the output of FF5 is LOW then FF6 subsequently returns LOW. FF6 returning LOW sets the output of FF5 momentarily HIGH and in doing so loads data from Register 6 into Register 5. This process is repeated down the stack until the input data reaches Register 1, FF1 going HIGH and remaining HIGH. Note that the SAMT flag, which was set HIGH after the Reset $\overline{RST}$, is unchanged. Register 1 is now no longer affected by subsequent write operations. Although all the other Stack Registers have the data of Register 1 in them, their control flip-flops are Low hence this data can be overwritten. The next Write operation initiates a similar sequence of events with data falling through to Register 2. The SAMT flag now goes LOW. After four further Write operations, the SFUL flag is set HIGH indicating the stack is full. See Table 2 and Functional Block Diagram.

By exercising $\overline{RLEN}$ and RL the output of the FF1 Control flip-flop is reset LOW. Register 1 will now appear empty and a roll-down sequence similar to that described above is initiated automatically. The data originally in Register 1 is lost and the SFUL flag is reset LOW. See Table 3 and Figure 1. Although not shown in Table 2 or Table 3 any arbitrary sequence of stack Write and Roll operations is permissible.

Data from Register 1 or Register 2 (selected by W1/$\overline{W2}$ control) may be loaded into the 12-bit DAC Register by exercising LDAC. See Table 4 and Figure 2. Note that a load DAC operation does not affect word positions in the stack hence stack flags, SFUL and SAMT, remain unchanged. LDAC is a level-triggered (as opposed to edge-triggered) control signal.

WRITE TIMING

The ripple-through nature of the stack leads to an apparent time skew (or delay) between Write signals and valid input data. Due to this delay, the input data to the device need not be valid on the trailing edge of $\overline{WR}$ (the normal constraint when writing) but must be valid some time later, t_{WDS}. This point is illustrated in the Functional Block Diagram. Input data must remain valid for some time after t_{WDS} max to allow the input latches to settle with the correct data. The hold time has been specified from the trailing edge of $\overline{WR}$ to the minimum data settling time required—t_{WDH} min—thus incorporating the internal time skewing. See Functional Block Diagram.

SAMT FLAG TIMING

Referring to the AD7544 Functional Diagram, the Stack Almost Empty (SAMT) flag is derived from a five-input NOR gate monitoring control flip-flops FF2 through FF6. After a $\overline{RST}$ signal all control flip-flop outputs are reset LOW and the SAMT flag is HIGH. When the first 12-bit word is written to the top of the stack, Register 6 control flip-flop momentarily goes HIGH as previously explained. The SAMT flag will go LOW and remain LOW while the word propagates down the stack. When the input data is finally latched in the Register 1 position, flip-flops FF2 through FF6 are again LOW and the SAMT flag will return HIGH. When the second word is written to the top of the stack, SAMT goes LOW and remains LOW since the word will fall-through to Register 2, FF2 going HIGH and remaining HIGH. Notice that SAMT flag behavior is dependent upon the Write frequency. If the time between Write cycles is less than the stack propagation delay (typ 2μs), then the SAMT flag will go LOW after the first $\overline{WR}$ signal and remain LOW since the next word will start falling-through before the first word has reached Register 1. If the SAMT flag is used as an interrupting input to the system microprocessor (rising edge triggered), the interrupt input should be masked during writing to avoid an erroneous interrupt call. During roll operations the interrupt mask should be removed since there is no possibility of glitches on the flag output.

STACK OPERATIONS—WRITING TO THE FIFO STACK

Operation	FIFO Stack Control Inputs					Data Input	Resulting Stack Register Contents						Output Flags	
	$\overline{RLEN}$	$\overline{RL}$	$\overline{WREN}$	$\overline{WR}$	$\overline{RST}$	D0–D11	R6	R5	R4	R3	R2	R1	SFUL	SAMT
Clear DAC Latch, Reset Stack F/Fs	X	X	X	X	0	X	Ⓧ	Ⓧ	Ⓧ	Ⓧ	Ⓧ	Ⓧ	0	1
Write Word A into Stack	1	X	0	↑	1	A	Ⓐ	Ⓐ	Ⓐ	Ⓐ	Ⓐ	A	0	1
Write Word B into Stack	1	X	0	↑	1	B	Ⓑ	Ⓑ	Ⓑ	Ⓑ	B	A	0	↓
Write Word C into Stack	1	X	0	↑	1	C	Ⓒ	Ⓒ	Ⓒ	C	B	A	0	0
Write Word D into Stack	1	X	0	↑	1	D	Ⓓ	Ⓓ	D	C	B	A	0	0
Write Word E into Stack	1	X	0	↑	1	E	Ⓔ	E	D	C	B	A	0	0
Write Word F into Stack	1	X	0	↑	1	F	F	E	D	C	B	A	↑	0
Write Word G into Stack	1	X	0	↑	1	G	F	E	D	C	B	A	1	0

NOTES
1 indicates logic HIGH
0 indicates logic LOW
X indicates "don't care"
Ⓧ, Ⓐ, Ⓑ etc. indicates data which can be overwritten
↑ indicates LOW to HIGH transition
↓ indicates HIGH to LOW transition

Table 2. Truth Table for Stack Write Operations

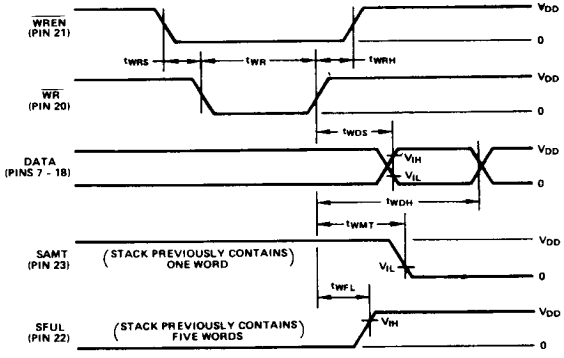


Figure 1. Timing Diagram for Write Operations

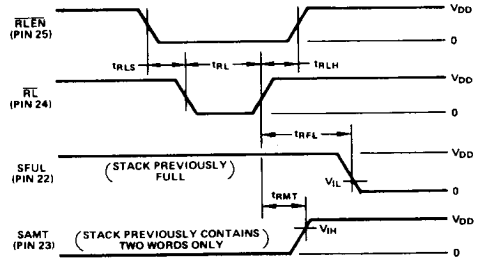


Figure 2. Timing Diagram for Stack Roll Operations

ROLLING THE FIFO STACK

Operation	FIFO Stack Control Inputs					Data Input	Resulting Stack Register Contents						Output Flags	
	$\overline{RLEN}$	$\overline{RL}$	$\overline{WREN}$	$\overline{WR}$	$\overline{RST}$	D0 - D11	R6	R5	R4	R3	R2	R1	SFUL	SAMT
Roll Down[1]	0	↑	1	X	1	X	Ⓕ	F	E	D	C	B	↓	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	F	E	D	C	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	F	E	C	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	F	E	0	0
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	F	0	↑
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	0	1
Roll Down	0	↑	1	X	1	X	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	Ⓕ	0	1

Note
[1] Initially stack registers R1 to R6 contain words A to F respectively.
See Table 2 notes.

Table 3. Truth Table for Stack Roll Operations

LOADING THE DAC

Operation	DAC Control Inputs W1/$\overline{W2}$	LDAC	$\overline{RST}$	DAC Output
Load DAC Register with all "0"s	X	X	0	Unipolar Mode; Output Assumes 0V Bipolar Mode; Output Assumes $-V_{REF}$
Load DAC Register from Word 1 Register	1	1	1	DAC Converts Word 1
Load DAC Register from Word 2 Register	0	1	1	DAC Converts Word 2

Table 4. Truth Table for DAC Register Loading

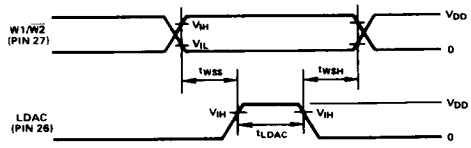


Figure 3. Timing Diagram for DAC Register Loading

NOTE: All input signal rise and fall times measured from 10% to 90% of V_{DD}, $t_r = t_f = 20ns$. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$

APPLYING THE AD7544

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 2, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 5.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Phase compensation capacitor C1 (10 to 25pF) may be required for stability when using high speed amplifiers. This capacitor cancels the pole formed by the DAC internal feedback resistance and output capacitance at OUT1.

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest. Bias current causes an output offset at V_{OUT} equal to I_B times the DAC feedback resistance (nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}, and low I_B.

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 5. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table 6 illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

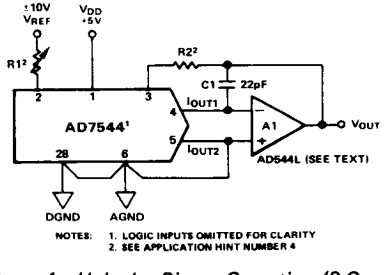


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

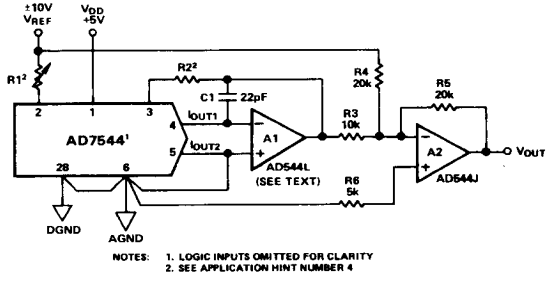


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 and 2R3 causes Full Scale error. C1 phase compensation (10 to 25pF) may be required for stability.

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 6. Bipolar Code Table for Offset Binary Circuit of Figure 5

CRT VECTOR GENERATION

The AD7544 can be used for vector generation in real-time CRT displays and intelligent X-Y plotters. Figures 6 and 7 show the waveforms and circuitry for a vector stroke or vector refresh display which generates a graphic display vector by vector. This is achieved by adding a linear ramp voltage to each starting point coordinate; the amplitude of this ramp being the difference between the start and finish coordinates of the vector. Two AD7544s are required for each axis. The fifth AD7544 in Figure 7 controls the CRT Z-mod input to vary the vector intensity with vector length; the intensity data having been previously computed.

Consider the two X-channel FIFO Registers of XDAC1 and XDAC2 to be simultaneously loaded with X axis coordinates. Word 1 (X1) of XDAC1 and Word 2 (X2) of XDAC2 are selected via the hard wired W1/$\overline{W2}$ control inputs. Hence the A1 output, after loading the DAC registers is,

$$V_{OX} = -X1\ (V_{REF1}) - X2\ (V_{REF2})$$

V_{REF1} and V_{REF2} are the reference voltages for XDAC1 and XDAC2 respectively;

$$V_{REF1} = V_{FS} - V(t)$$

and $V_{REF2} = V(t)$

where V_{FS} is the required full scale output voltage and V(t) is a positive ramp voltage of period T and maximum amplitude of V_{FS}. See waveforms of Figure 6.

Now $V_{OX} = -X1\ (V_{FS}) + V(t)\ (X1 - X2)$
at t = 0; V(t) = 0

and $V_{OX} = -X1\ (V_{FS})$

at t = T; $V(t) = V_{FS}$

and $V_{OX} = -X2\ (V_{FS})$

Thus a vector has been generated between X1 and X2. To generate the next vector between X2 and X3 the reference ramp is reset, both AD7544 stacks are rolled and their DAC registers subsequently loaded. The output voltage is now

$$V_{OX} = -X2\ (V_{REF1}) - X3\ (V_{REF2})$$

Operation of the two Y-channel AD7544s is identical to the above. During vector generation the constant reference voltage to the Z-mod AD7544 is multiplied by the appropriate brightness data in its DAC register. During ramp resetting and DAC register loading the polarity of this reference voltage is changed causing screen blanking.

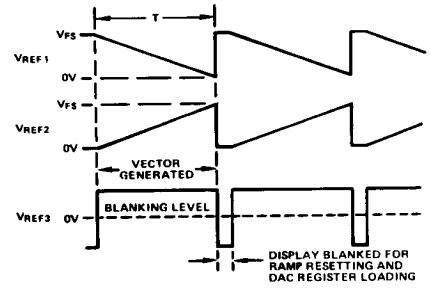


Figure 6. CRT Vector Generation Waveforms

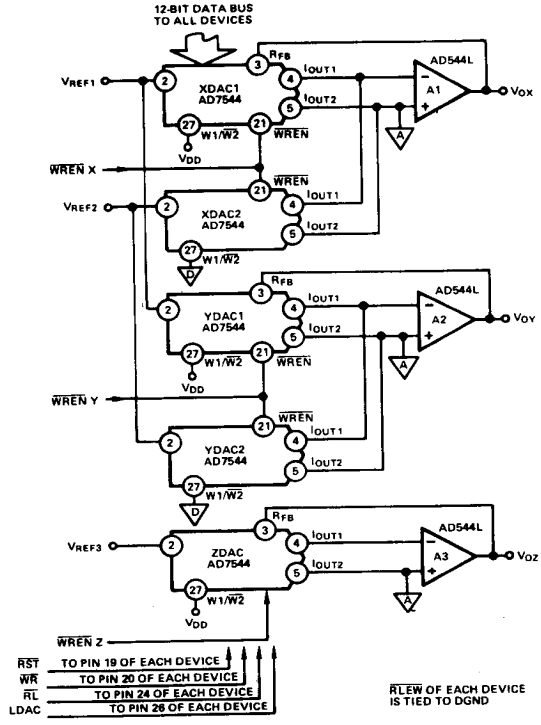


Figure 7. CRT Vector Generation Application

APPLICATION HINTS

The AD7544 is a precision 12-bit multiplying DAC designed for system interface. For a detailed description of multiplying DACs the reader is referred to Analog Devices "Application Guide to CMOS Multiplying D/A Converters". To ensure system performance consistent with AD7544 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7544 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7544. In more complex systems where the AGND – DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7544 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output of magnitude $0.67V_{OS}$ (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended the amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7544 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7544 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 5 and 6 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7544 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm/°C}$$

However, if the "G" version of the AD7544 is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C.