National Semiconductor

LM1880 No-Holds Vertical/Horizontal

General Description

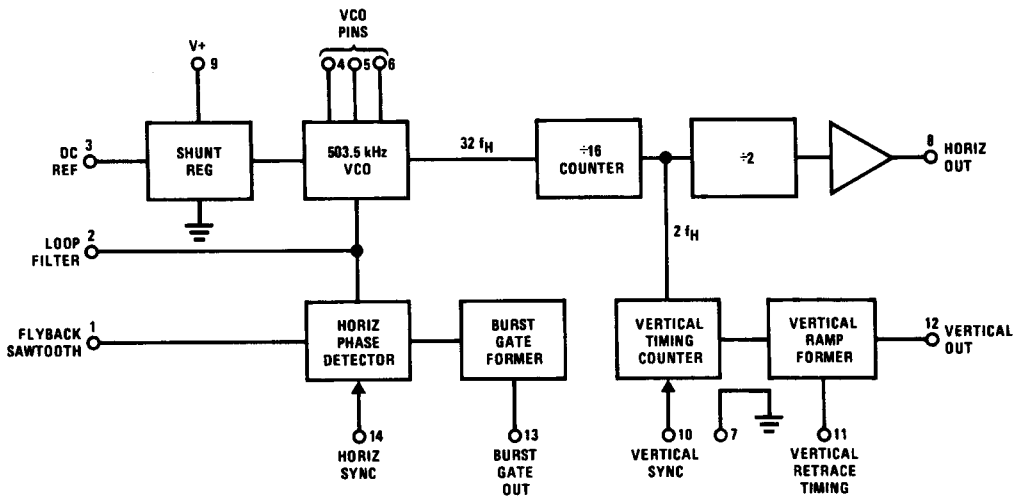
The LM1880 uses compatible Linear/I^2L technology to produce the first T.V. horizontal and vertical processing system which completely eliminates the hold controls. The heart of the system is a precision 32 times horizontal frequency VCO which is designed to use a low-cost ceramic resonator as a tuning element.

The VCO signal is divided down in the horizontal section to produce a pre-driver output which is locked to negative sync by means of an on-chip phase detector. The vertical output ramp is injection-locked by vertical sync subject to a sync window derived from the vertical countdown section. A gate pulse centered on the chroma burst is also provided.

Features

- No frequency set-up required for horizontal or vertical
- Ceramic resonator frequency reference
- Accurate horizontal pre-driver duty cycle
- Vertical sync window referenced to horizontal
- Precise interlaced vertical output
- APC loop parameters completely adjustable
- Vertical retrace time adjustable
- Chroma burst gate output
- Internal voltage regulator
- Improved vertical lock time

Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Current (Pin 9)	40 mA
Output Voltage (Pins 8, 12, 13)	12V
Output Current	
Pin 8	50 mA
Pin 12	15 mA
Pin 13	10 mA
Sync. Input Voltage (Pins 10, 14)	5 Vp-p
Sawtooth Input Voltage (Pin 1)	5 Vp-p
Package Dissipation, $T_A = +25°C$	1400 mW
Above $T_A = 25°C$, Derate Based on $T_{J(MAX)} = +150°C$ and $\theta_{JA} = +90°C/W$	
Storage Temperature Range	$-55°C$ to $+150°C$
Operating Temperature Range	$0°C$ to $+70°C$
Lead Temperature (Soldering, 10 sec.)	$+260°C$

Electrical Characteristics (Test Circuit, all SW normally pos. 1, $T_A = 25°C$, $V^+ = 12V$)

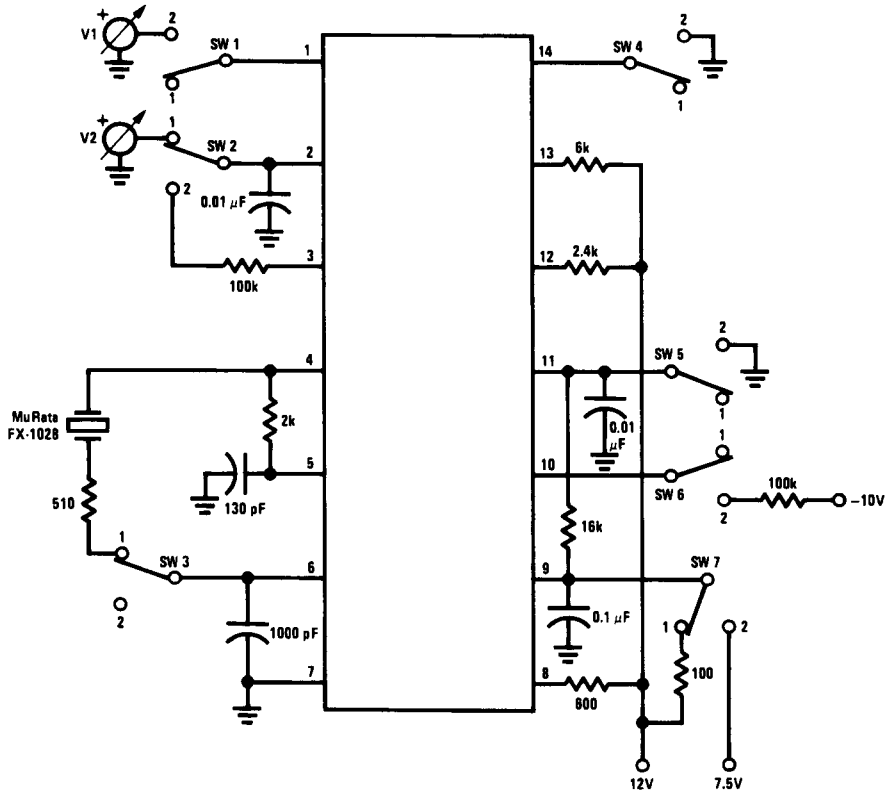
Parameter	Conditions	Min	Typ	Max	Units
Regulated Voltage (Pin 9)		8.2	8.7	9.2	V
Supply Current (Pin 9)	SW 7 Pos. 2, $V_9 = +7.5V$	12	18	24	mA
VCO Reference Voltage (Pin 3)			5.1		V
VCO Control Current (Pin 2)	V2 = 5V		0.25	1.0	μA
Horizontal Phase Detector Sink Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 3.9V, V2 = 5V	0.3	0.5		mA
Horizontal Phase Detector Source Current (Pin 2)	SW 1, SW 4 Pos. 2, V1 = 1.9V, V2 = 5V	0.3	0.5		mA
Horizontal Output Leakage (Pin 8, OFF Condition)	Change SW 3 to Pos. 2 with Pin 8 High			150	μA
Horizontal Output Saturation Voltage (Pin 8, ON Condition)	Change SW 3 to Pos. 2 with Pin 8 Low		0.15	0.4	V
Vertical Output Saturation Voltage (Pin 12)	SW 3, SW 5 Pos. 2		0.25	0.5	V
Burst Gate Saturation Voltage (Pin 13)	SW 1, SW 4 Pos. 2, V1 = 1.9V		0.15	0.4	V
Horizontal Oscillator Free-Running Frequency (Pin 8), (Note 1)	SW 2 Pos. 2	15,550	15,750	15,950	Hz
Horizontal Oscillator Maximum Frequency (Pin 8)	V2 = 7V	16,300			Hz
Horizontal Oscillator Minimum Frequency (Pin 8)	V2 = 3V			15,150	Hz
Vertical Minimum Lock Frequency (Pin 12)	$f_H = 15,734$ Hz			55.0	Hz
Vertical Maximum Lock Frequency (Pin 12)	SW 6 Pos. 2, $f_H = 15,734$ Hz	61.7			Hz

Note 1: Assumes ceramic resonator $f_R = 503.48$ kHz.

Design Parameters (Application Circuit)

Parameter	Conditions	Min	Typ	Max	Units
Horizontal Pull-In Range			±600		Hz
Horizontal Static Phase Error (S.P.E.)	$\Delta f_H = \pm 600$ Hz		±0.5		μs
Horizontal Output Duty Cycle			50		%
Horizontal Oscillator Supply Sensitivity			−1		Hz/V
Vertical Output Retrace Time			600		μs
Burst Gate Width	Flyback Width = 12 μs		5		μs

Test Circuit



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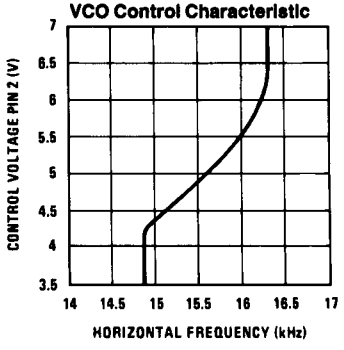
Order Number LM1880J
See NS Package Number J14A

Typical Performance Characteristics

VCO Control Characteristic



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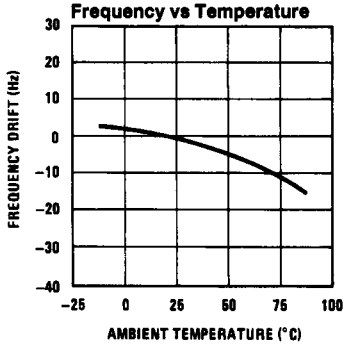
Horizontal Free-Running Frequency vs Temperature



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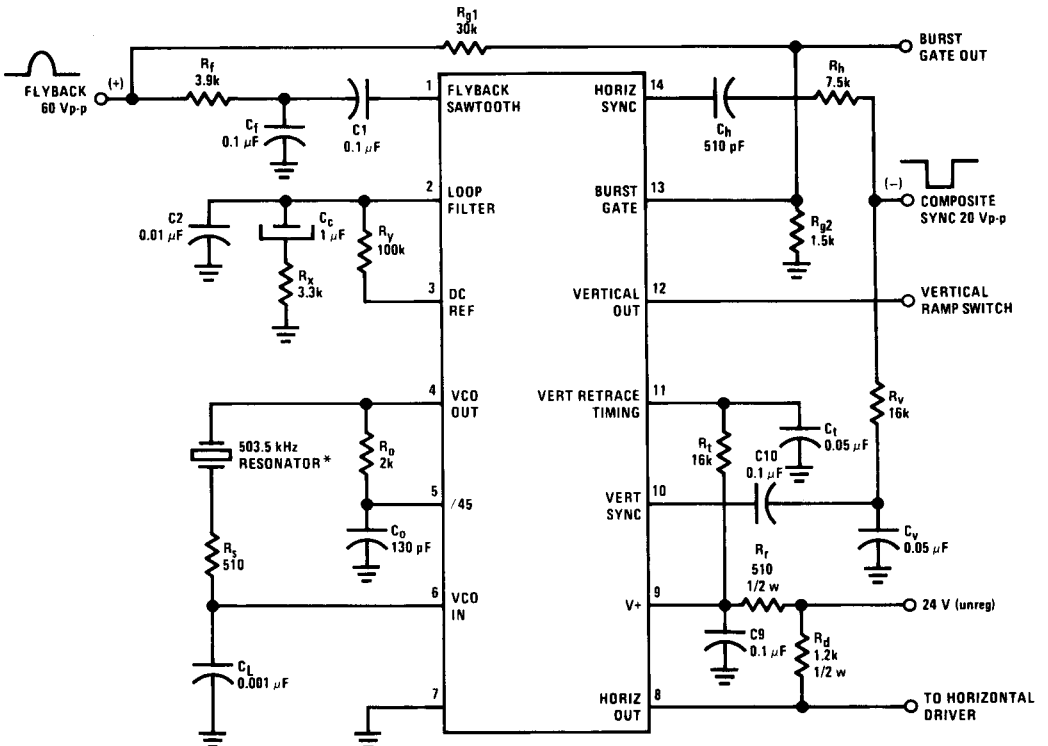
Typical Application



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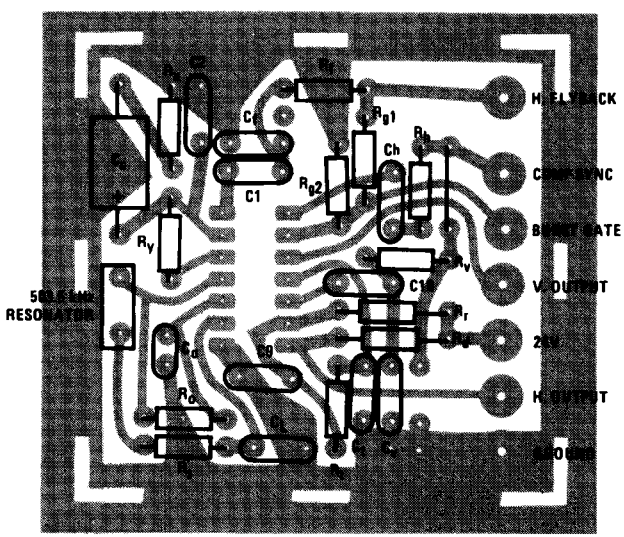
*MuRata Corporation of America, Part No. CSB503B

Printed Circuit Layout

(COMPONENT SIDE)



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External Components (Application Circuit)

Component	Typical Value	Comments
R_{g1}	30k	Burst Gate series resistor.
R_{g2}	1.5k	Burst Gate shunt resistor, works with R_{g1} to divide flyback pulse and set Burst Gate amplitude. $V_{B.G.pk} = \frac{R_{g2}}{R_{g1} + R_{g2}} V_{FLYBACK}$
R_f	3.9k	Flyback Sawtooth integrator resistor, works with C_f to integrate flyback pulse to 1 Vp-p min sawtooth. For $C_f = 0.1\ \mu F$, $V_{SAW\ p\text{-}p} \cong \frac{85 V_{FLYBACK}}{R_f}$
C_f	0.1 μF	Flyback Sawtooth integrator capacitor.
C1	0.1 μF	Sawtooth input coupling capacitor.
R_h	7.5k	Horizontal Sync input coupling resistor. $R_h = 0.4 \times V_{SYNC\ p\text{-}p}\ k\Omega$
C_h	510 pF	Horizontal Sync input coupling capacitor, blocks vertical sync components.
R_v	16k	Vertical sync input integrator resistor.
C_v	0.05 μF	Vertical sync input integrator capacitor, works with R_v to integrate composite sync to -2 Vp-p min pulse. For N.T.S.C. sync, Vert. sync $\cong \frac{1.4 \times 10^{-4}}{R_v C_v}$ (Comp. sync) Vp-p
C10	0.1 μF	Vertical sync coupling capacitor.
R_t	16k	Vertical Retrace timing resistor.
C_t	0.05 μF	Vertical Retrace timing capacitor, works with R_t to determine ON time of vertical ramp switch at pin 12. t_V. RETRACE $\cong 0.75\ R_t C_t$ sec.
R_o	2k	Oscillator phase shift resistor.
C_o	130 pF	Works with R_o to produce 45° lag required by VCO phase shifter.
R_s	510Ω	Defines Q of ceramic resonator tuned network, which affects VCO control curve.
C_L	1000 pF	Completes VCO loop with phase lag, required to sustain oscillation and suppress resonator overtones.
R_r	510Ω	Series resistor to device supply pin 9. Must supply sufficient current to activate internal shunt regulator. $R_r = \frac{V_{(unreg)} - 9V}{0.03}\ \Omega$
C9	0.1 μF	Device supply decoupling capacitor.
R_d	1.2k	Horizontal pre-driver output resistor, supplies base current to Horizontal driver transistor when pin 8 is OFF.
C2	0.01 μF	Horizontal APC loop filter high frequency roll-off. C2 also prevents signal on loop filter from saturating phase detector output.
R_x	3.3k	R_x, R_Y and C_c form the Horizontal APC loop filter. See Applications Information to modify loop parameters.
R_y	100k	
C_c	1 μF	

Applications Information

I. VERTICAL COUNTER

The vertical counter in the LM1880 replaces the conventional vertical oscillator in a television receiver. The vertical lock-in range is governed by the width of the vertical sync window, which opens from count 510 to count 574 following a vertical reset. The vertical lock frequencies are referenced to twice horizontal frequency to insure interlaced vertical and horizontal outputs. For f_{HORIZ} = 15,734 Hz, the vertical lock frequencies are calculated as follows:

$$f_{V.HIGH} = \frac{2\,(15{,}734)}{510} = 61.7\ \text{Hz}.$$

$$f_{V.LOW} = \frac{2\,(15{,}734)}{574} = 54.8\ \text{Hz}.$$

In virtually all standard and non-standard sync signals the vertical sync is also derived from the horizontal, so that as long as the horizontal sync frequency is within the pull-in range of the LM1880 (approximately ±600 Hz), the vertical lock window will remain centered on the vertical sync. Thus, the effective vertical lock range is increased by the horizontal APC:

$$f_{V.HIGH(EFF)} = \frac{2\,(15{,}734 + 600)}{510} = 64\ \text{Hz}.$$

$$f_{V.LOW(EFF)} = \frac{2\,(15{,}734 - 600)}{574} = 52.7\ \text{Hz}.$$

The time required for the vertical to "roll-thru" and lock is a function of the difference frequency and relative phase of $f_{V.LOW}$ and the vertical sync:

$$t_{ROLL\text{-}THRU\ (AVG)} = \frac{1}{2}\,\frac{1}{60 - 55\ \text{Hz}} = 100\ \text{ms}.$$

II. HORIZONTAL APC LOOP PARAMETERS

The following information is given to provide a basis for modifying the filter to achieve the desired loop performance. Although the VCO is actually running at 503.5 kHz, for convenience all parameters are referenced to the actual horizontal output frequency at pin 8.

DC Loop Gain

The DC loop gain is the product of the phase detector conversion gain (μ) and the VCO sensitivity (β). For the typical application circuit,

$\mu = 1.6 \times 10^{-4}\, R_y$ V/Rad

and

β = 800 Hz/V

$\mu\beta = 0.13\, R_y$ Hz/Rad

for R_y = 100 kΩ, $\mu\beta$ = 13,000 Hz/Rad

In order to determine static phase error (S.P.E.), the loop gain may be expressed in Hz/μs:

$$\mu\beta = \frac{13{,}000 \times 2\pi}{63.5\ \mu\text{s}} = 1{,}286\ \text{Hz}/\mu\text{s}$$

For comparison, this value is nearly double the loop gain of the LM1391. The increased loop gain (reduced phase error) guarantees accurate centering of the burst gate pulse on pin 13 of the LM1880.

The following equations cover AC loop parameters of interest:

Noise Bandwidth

$$f_{NN} \cong \frac{1 + 2\pi\,(R_x^2/R_y)\,C_C\,\mu\beta}{4R_xC_C}\ \text{Hz}.$$

Damping Factor

$$K \cong \frac{\pi}{2}\,\frac{R_x^2}{R_y}\,C_C\,\mu\beta$$

Pull-In Range

The pull-in and hold-in range of the LM1880 horizontal APC loop are directly determined by the VCO control range. Thus the loop would be capable of pulling the VCO further than ±600 Hz, but it has well defined frequency limits which prevent it from doing so. As a result of these built-in "stops", the loop parameters may be varied over a large range without affecting pull-in performance.

The VCO control range, and hence pull-in, can be modified to some extent by varying the Q of the ceramic resonator with resistor R_S:

Incr. R_S → Incr. Pull-in
Reduce R_S → Reduce Pull-in

However, because of the non-linearity of the resonator, R_S has a much greater effect on the negative side pull-in than the positive side.

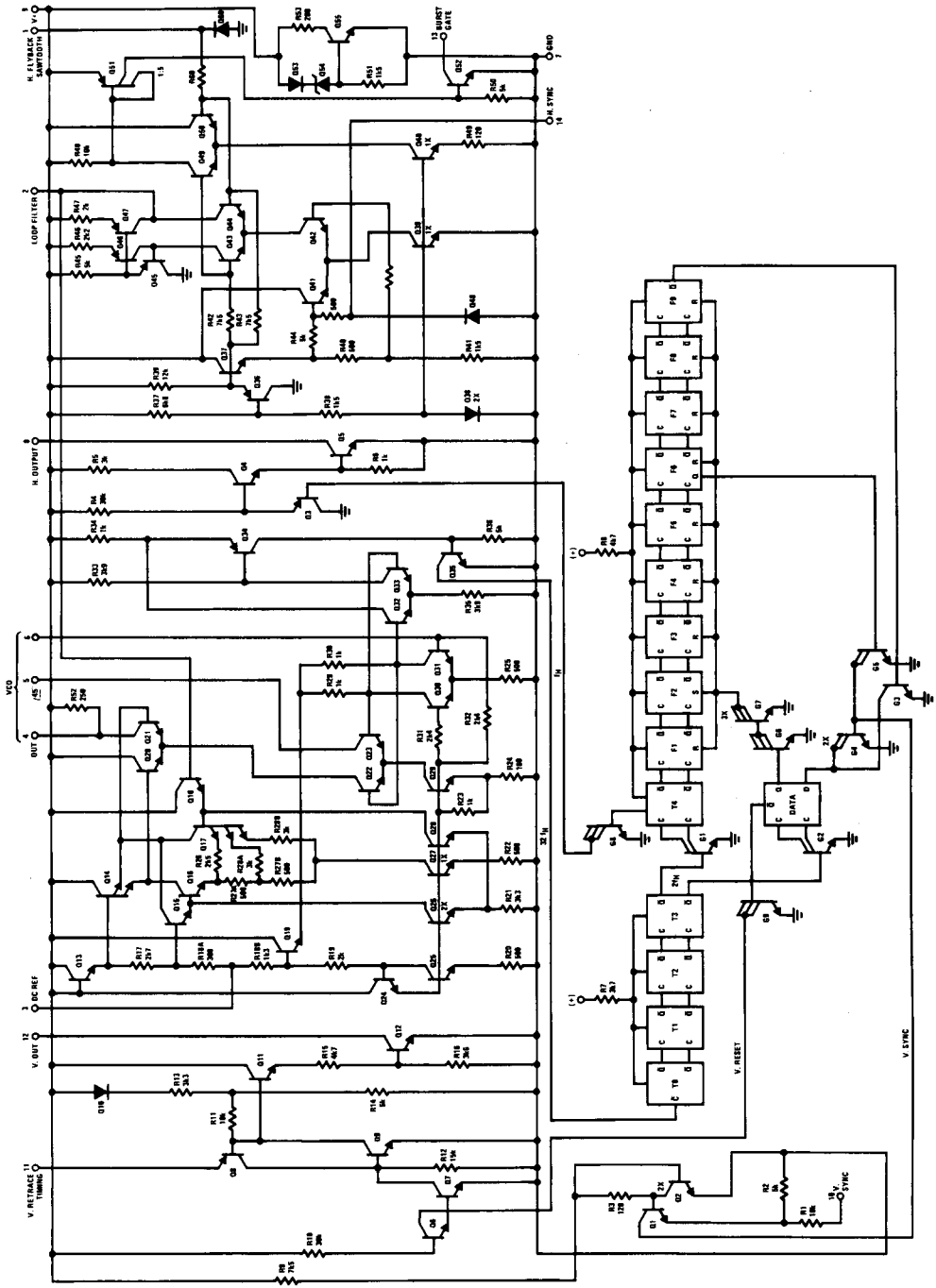
III. LAYOUT NOTES

Since the LM1880 uses a counter to derive the horizontal frequency, care must be taken to prevent extraneous signals from the horizontal driver and output stages from feeding back to the VCO where they could cause false counts and consequent severe phase jitter. The following guidelines will prevent this problem from occuring:

A. Keep the VCO feedback capacitor, C_L, as close as possible to device pins 6 and 7.

B. Limit the lead length on the horizontal output pin 8. If a long line is required to the driver base, isolate it with a small series resistor (200–300Ω) next to pin 8.

Schematic Diagram



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Circuit Description (See Schematic Diagram)

The LM1880 uses a phase-shift type voltage-controlled oscillator (VCO). The gain for the oscillator loop is derived from differential amplifiers Q30, Q31 and Q22, Q23. The collector current in Q23 is phase-shifted 45° at pin 5 and summed with a portion of the current in Q22, controlled by differential amplifier Q20, Q21. The resulting output phase at pin 4 coupled through the ceramic resonator to pin 6 defines the oscillation frequency. Differential amplifier Q16, Q17, controlled by the pin 2 voltage, determines the current split in Q20 and Q21 and, consequently, the pin 4 phase and oscillation frequency. The multiple-emitter degeneration in Q17 compensates the resonator phase characteristic to produce a nearly linear VCO control curve.

The 503.5 kHz output of the VCO is taken from squaring amplifier Q32, Q33 through Q34 and Q35 to the $I^2L \div 16$ pre-scaler T0–T3. The $2f_H$ output is then divided again in T4 to produce the desired horizontal frequency at gate G8. The horizontal pre-driver section consists of Q3, Q4 and Q5, which produce an open-collector output square-wave at pin 8.

The $2f_H$ pre-scaler output also drives a data flip-flop which resets the vertical counter F1–F9. The data input of the reset flip-flop is controlled by the vertical sync from pin 10 subject to gates G3 and G5. After 510 $2f_H$ cycles following reset, vertical sync from Q1 and G4 is enabled by G3. A sync pulse received after this time initiates reset on the next $2f_H$ cycle. If no pulse is received after 542 cycles, G5 will initiate the reset process. A reset pulse from the counter is taken via G9 to the retrace timing section. SCR Q8, Q9 is normally ON, holding a capacitor on pin 11 near ground. During this time Q11 and Q12 are OFF, allowing the vertical ramp to form on pin 12. When the reset pulse is received, Q7 turns Q8, Q9 OFF and Q11, Q12 ON, discharging the vertical ramp for the duration of the retrace time. Retrace is completed when the pin 11 capacitor charges to the Q8 threshold, and the SCR again latches.

The remaining sections of the device are the horizontal phase detector and burst gate former. The balanced phase detector consists of comparator Q43, Q44 and current source Q39 gated by differential amplifier Q41, Q42. Negative horizontal sync pulses on pin 14 enable the comparator, and the flyback sawtooth on pin 1 switches the current from Q43 to Q44 based on the relative phase between the sync and sawtooth. Q44 takes a (−) current pulse from pin 2, while the pulse in Q43 is turned around in the current mirror Q45, Q46 and Q47 to produce a (+) current pulse at pin 2. These currents are then integrated by the external loop filter to control the VCO.

The flyback sawtooth also switches differential amplifier Q49, Q50, which activates the burst gate. During the first half of the flyback pulse Q49 will be ON, which turns Q51 and Q52 ON and clamps pin 13 near ground. The sawtooth switches Q49, Q51 and Q52 OFF at the peak of the flyback, releasing pin 13. In this manner, the second half of a flyback pulse fed to pin 13 can be used as a burst gate.

Q53, Q54 and Q55 form the active shunt regulator which holds the supply pin 9 at 8.7V typ.