

4204 4206

# **ANALOG MULTIPLIER-DIVIDER**

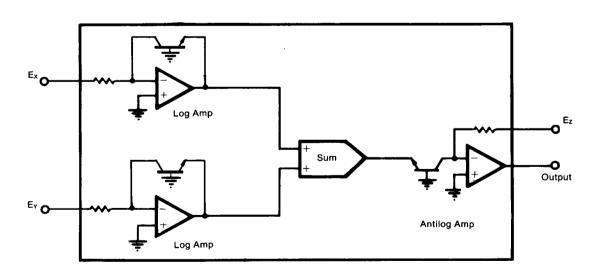
# **FEATURES**

- HIGH TOTAL ACCURACY
   0.25% and 0.5% max, no external trims
   0.1% and 0.2% typ. with external trims
- LOW TEMPERATURE DRIFT 100ppm/°C
- SMALL PACKAGE
   Dual-in-line metal or plastic
- LOW COST

# DESCRIPTION

The 4204 and 4206 are four-quadrant analog multipliers offering high accuracy, low noise, and moderate

bandwidth at low cost. They use the log/antilog technique and are internally laser-trimmed. Multiply mode accuracies of 0.25% and 0.5% max are guaranteed with no external components. By following the external trim procedure described in the Multiplication section, accuracies can be improved to 0.1% and 0.2% (typical). Accuracy specifications are verified at Burr-Brown by an automatic tester which scans the X-Y plane. Maximum error at any point in the plane is required to be less than the specified values. The 4204 and 4206 also perform the divide function in two quadrants and the square root function in one quadrant with no external components required. Detailed instructions for these operations are given on the last page.



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# **SPECIFICATIONS**

#### **ELECTRICAL**

Typical performance at +25°C with rated power supplies unless otherwise noted. Percent specifications refer to percent of full scale (10V).

MODEL	4204J, 4206J	4204K, 4206K	4204\$
OUTPUT FUNCTION	E <sub>x</sub> E <sub>y</sub> / 10		*
TOTAL ERROR (Multiply Mode) <sup>(1)</sup> Internal trim, max <sup>(2)</sup> External trim. typ vs Temperature vs Supply	0.5% max 0.2% 0.01%/°C 0.02%/%	0.25% max 0.1% * *	* 0.1% 0.02%/°C max *
INDIVIDUAL ERRORS (Multiply Mode) Output Offset X = Y = 0 Scale Factor Error Nonlinearity: X = 20V, p-p, Y = -10VDC Y = 20V, p-p, X = -10VDC X = 20V, p-p, Y = +10VDC	15mV 0.2% 0.005% 0.005% 0.05%	5mV 0.1% * *	5mV 0.1% * *
X = 20V, p-p, X = +10VDC X = 20V, p-p, X = +10VDC Feedthrough at 50Hz: X = 20V, p-p, Y = 0 Y = 20V, p-p, X = 0 AC PERFORMANCE	0.05% 0.05% 10mV, p-p 10mV, p-p	•	5mV, p-p 5mV, p-p
Slew Rate  —3dB Small Signal Bandwidth  1% Amplitude Error  1% Vector Error (0.57° phase shift) Full Power Response	1V/µs 250kHz 33kHz 2.5kHz 20kHz	* * *	* * * *
OUTPUT NOISE X = Y = 0.0V DC to 10kHz	300μV, rms	*	*
INPUT CHARACTERISTICS Input Voltage:     Maximum for Rated Specifications X, Y, Z     Maximum Safe Level X, Y, Z Input Impedance X/Y/Z	±10V ±Supply 25kΩ/25kΩ/100kΩ	*	*
OUTPUT CHARACTERISTICS Rated Output: Voltage, min Current, min Output Impedance	±10V ±5mA 1Ω	*	*
POWER SUPPLY REQUIREMENTS Rated Supply Operating Range Quiescent Current	±15VDC ±14 to ±16V +15mA, -8.5mA	* * *	* *
TEMPERATURE RANGE, 4206 Specification Operating Storage	0°C to +70°C -25°C to +85°C -55°C to +125°C	* * *	
TEMPERATURE RANGE, 4204 Specification Operating Storage	-25°C to +85°C -55°C to +125°C -65°C to +125°C	* *	-55°C to +125°C * *

<sup>\*</sup>Same as for 4206J.

NOTES: (1) Total error is a tested maximum and does not represent a sum of the maximum individual errors as the maximum individual errors do not occur at the same X, Y operating point. (2) With output loading of  $10k\Omega$  or less.

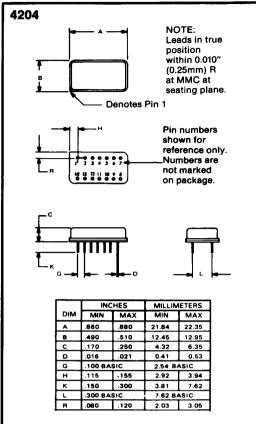
## **PIN CONNECTIONS 4204**

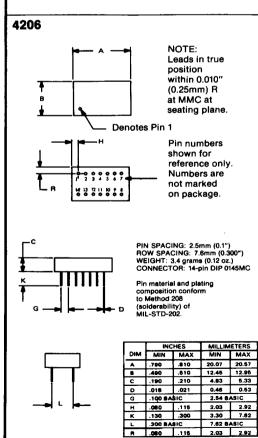
- 1 Ez
- 2 Output
- 3 -Vs
- 4 Feedthrough Adjust
- 5 Make No Connection
- 6 Make No Connection
- 7 E<sub>x</sub>
- 8 Internal Reference
- 9 Make No Connection
- 10 Ground
- 11 Feedthrough Adjust
- 12 Offset Adjust
- 13 E<sub>Y</sub>
- 14 +Vs

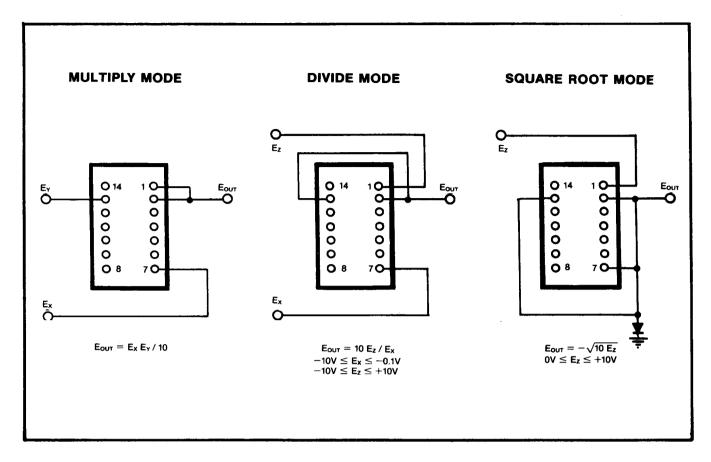
# PIN CONNECTIONS 4206

- Ez
- 2 Output
- 3 -Vs
- 4 Feedthrough Adjust
- 5 Make No Connection
- 6 Make No Connection
- 7 Ex
- 8 Internal Reference
- 9 Make No Connection
- 10 Ground
- 11 Feedthrough Adjust
- 12 Offset Adjust
- 13 E<sub>Y</sub> 14 +V<sub>S</sub>

#### **MECHANICAL**







#### **ADJUSTMENTS**

Although the products will achieve specified performance in the multiply mode with no external trimming, optimized performance can be achieved with external adjustments. The proper connections and the trim procedures are explained below.

The 4204 and 4206 will operate within specification with any combination of input signals. The best performance, however, will be obtained in the second, third, and fourth quadrants. That is, if four quadrant operations are not needed, the performance can be optimized by constraining operation to quadrants 2, 3 and 4 rather than 1.

# **MULTIPLICATION**

### **Multiplication Trim Procedure (Figure 1)**

- 1) Set  $E_X = 0$  and apply a 10Vp-p sine wave (50Hz) to  $E_Y$ : Adjust  $R_1$  for minimum output.
- 2) Set  $E_Y=0$  and apply a 10Vp-p sine wave (50Hz) to  $E_X$ : Adjust  $R_2$  for minimum output.
- 3) Set  $E_X = E_Y = 0$ : Adjust  $R_3$  for  $E_{OUT} = 0.00$ V.
- 4) Set  $E_X = E_Y = +10.000V \pm 1mV$ : Adjust  $R_4$  for  $E_{OUT} = +10.000V \pm 2mV$ .

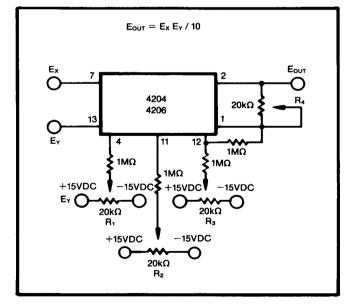


FIGURE 1. Multiplication Trim Procedure.

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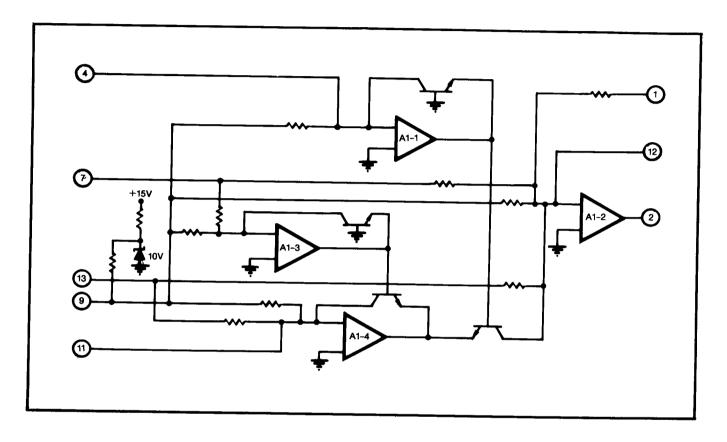
## **OUTPUT DISTORTION**

The output distortion of the 4204 and 4206 is of most interest in modulator applications. The curve for Output Distortion characterizes this distortion with one input held at +10 or -10VDC. A sine wave is applied to the other input. The sine wave amplitude is held constant at 20Vp-p while frequency is varied.

# **AC FEEDTHROUGH**

This variation of feedthrough as a function of frequency is illustrated in the curve above. One of the inputs is a zero while a 20Vp-p sine wave is applied at the other input. The output feedthrough generally has substantial harmonic content and is measured in millivolts, peak-to-peak.

# THEORY OF OPERATION



These products' log-antilog multiplication technique is based upon the logarithmic voltage-current relationship in a semiconductor junction. This action is shown by the simplified equation:

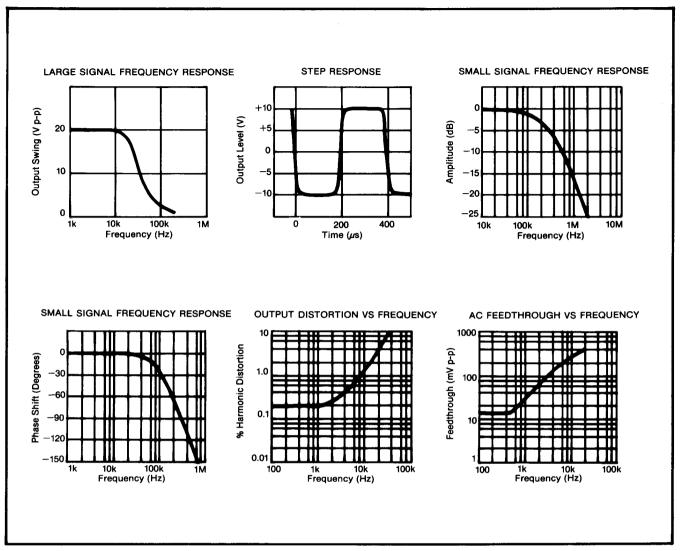
$$V_{BE} = (KT/q) (1n I_C - 1n I_S)$$

where  $V_{BE}$  is the transistor's emitter-base voltage,  $I_{\rm C}$  is the transistor collector current,  $I_{\rm S}$  is the collector saturation current, K is Bolzmann's constant, q is the charge of one electron and T is the absolute temperature in degrees Kelvin. As can be seen from the equation, the

logarithmic function is extremely temperature sensitive. The 4204 and 4206, however, have excellent temperature characteristics because the log and antilog circuitry have equal and opposite temperature drifts which cancel to a first order approximation. The log and antilog circuits will compensate each other to the extent that the various logging transistors are matched to each other. These transistors are placed adjacently on a monolithic chip to obtain the best possible matching, and so the best possible performance.

# **TYPICAL PERFORMANCE CURVES**

At +25°C and ±15VDC.



# DISCUSSION OF PERFORMANCE CURVES

# LARGE SIGNAL FREQUENCY RESPONSE

This response curve describes the output voltage capability of the 4204 and 4206 as a function of frequency. The measurement is made with one input at +10 or -10VDC, and with a sine wave applied at the other input. An output distortion of 0.5% is allowed.

# STEP RESPONSE

Step response is measured with one input at +10 or -10VDC and with a 20Vp-p square wave applied at the other input.

#### SMALL SIGNAL FREQUENCY RESPONSE

These curves are the amplitude and phase response of the 4204 and 4206's transfer function, when one input is held at +10 or -10VDC. A sine wave signal is applied to the other input. Small signal response requires that the amplitude of the input sine wave be adjusted so that the output signal does not reach the slew rate limitation.

#### DIVISION

The 4204 and 4206 may be used as a two-quadrant divider without the need for an external operational amplifier. It should, however, be noted that the maximum output error is approximately given by

divider error 
$$\approx 10 \varepsilon_{\rm M} / E_{\rm X}$$

where  $\varepsilon_{\rm M}$  is the total error specification for the multiply mode. Obviously, divider error becomes excessively large for small values of  $E_{\rm X}$ . A 10:1 denominator range is usually the practical limit. If accurate division is required over a wide dynamic range of denominator voltage, the Burr-Brown Model DIV100 is recommended (0.25% max., over a 40:1 range).

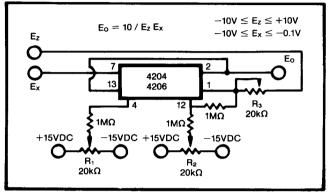


FIGURE 2. Division Trim Procedure.

### **Division Trim Procedure (Figure 2)**

- 1) Set all potentiometers near mid-scale.
- 2) Set  $E_Z = 0V$ ,  $E_X \approx -10V$ , adjust  $R_2$  such that  $E_0 = 0.000V \pm 2mV$ .
- 3) Set  $E_X = E_Z = -10.000 \text{VDC} \pm 2 \text{mV}$ , adjust  $R_3$  such that  $E_0 = +10.000 \text{VDC} \pm 2 \text{mV}$ .
- 4) Set  $E_X = E_Z \approx$  minimum value required by application, adjust  $R_1$  such that  $E_0 = +10.000 \text{VDC} \pm 5 \text{mV}$ .
- 5) Repeat steps 2 through 4 if necessary.

#### **SQUARE ROOT**

The pin connections for the Square Root mode of operation are similar to those for division, except that the denominator input is connected to the output node. Errors in the Square root mode of operation become troublesome for small values of  $E_{\rm Z}$ . However, the output error does not increase so rapidly as in the divide mode. The actual output for small values of  $E_{\rm Z}$  is given approximately by

$$E_{OUT} \approx -\sqrt{10} E_z + 10 \varepsilon_M$$

where  $\varepsilon_{\rm M}$  is the total error specifed for Multiply mode. This equation can be used to determine the feasibility of using either of these products as a square rooter for a given application. For operation over a much wider dynamic range, with improved accuracy, the Model 4302 multifunction converter is recommended.

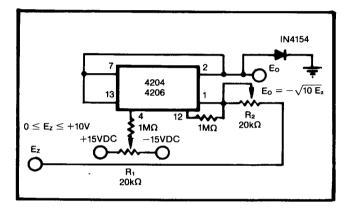


FIGURE 3. Square Root Trim Procedure.

# **Square Root Trim Procedure (Figure 3)**

- 1) Set  $E_z = \pm 10.000 \text{VDC} \pm 2 \text{mV}$ , adjust  $R_2$  such that  $E_0 = \pm 10.000 \text{VDC} \pm 2 \text{mV}$ .
- 2) Set  $E_Z \approx \text{minimum}$  value required by application  $(E_{ZM})$ , adjust  $R_1$  such that  $E_O = -\sqrt{10 \ E_{ZM}} \pm 2 \text{mV}$ .
- 3) Repeat steps 1 and 2 if necessary.

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