



DAC0800/DAC0801/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in Figure 1. The reference-to-full-scale current matching of better than ± 1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than $\pm 0.1\%$ over temperature minimizes system error accumulations.

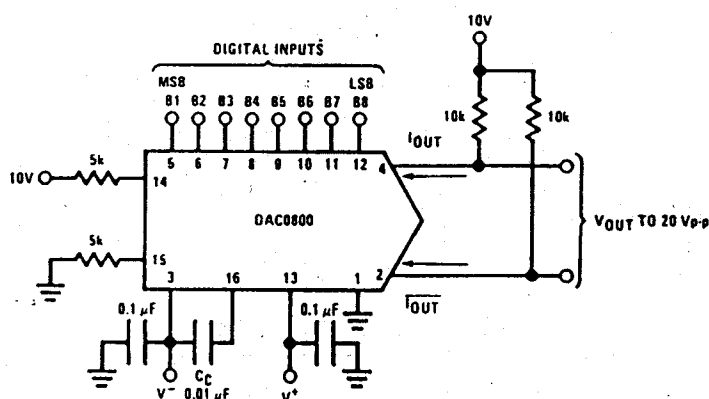
The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC} , grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full $\pm 4.5V$ to $\pm 18V$ power supply range; power dissipation is only 33 mW with $\pm 5V$ supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C, DAC0801C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, DAC-08E and DAC-08H, respectively.

Features

- Fast settling output current 100 ns
- Full scale error ± 1 LSB
- Nonlinearity over temperature $\pm 0.1\%$
- Full scale current drift ± 10 ppm/ $^{\circ}C$
- High output compliance $-10V$ to $+18V$
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range $\pm 4.5V$ to $\pm 18V$
- Low power consumption 33 mW at $\pm 5V$
- Low cost

Typical Applications



TL/H/5686-1

FIGURE 1. ± 20 Vp-p Output Digital-to-Analog Converter (Note 4)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A)*		N Package (N16A)*		SO Package (M16A)
$\pm 0.1\%$ FS	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	DAC0802LJ	DAC-08AQ	DAC0802LCN	DAC-08HP	DAC0802LCM
$\pm 0.1\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	DAC0802LCJ	DAC-08HQ			
$\pm 0.19\%$ FS	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	DAC0800LJ	DAC-08Q	DAC0800LCN	DAC-08EP	DAC0800LCM
$\pm 0.19\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	DAC0800LCJ	DAC-08EQ			
$\pm 0.39\%$ FS	$0^{\circ}C \leq T_A \leq +70^{\circ}C$	DAC0801LCJ	DAC-08CQ	DAC0801LCN	DAC-08CP	DAC0801LCM

*Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	$\pm 18V$ or $36V$
Power Dissipation (Note 2)	500 mW
Reference Input Differential Voltage (V_{14} to V_{15})	V^- to V^+
Reference Input Common-Mode Range (V_{14}, V_{15})	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^- plus $36V$
Analog Current Outputs ($V_S = -15V$)	4.25 mA
ESD Susceptibility (Note 3)	TBD V
Storage Temperature	$-65^\circ C$ to $+150^\circ C$

Lead Temp. (Soldering, 10 seconds)

Dual-In-Line Package (plastic) $260^\circ C$

Dual-In-Line Package (ceramic) $300^\circ C$

Surface Mount Package

Vapor Phase (60 seconds) $215^\circ C$

Infrared (15 seconds) $220^\circ C$

Operating Conditions (Note 1)

	Min	Max	Units
Temperature (T_A)			
DAC0802L	-55	$+125$	$^\circ C$
DAC0800L	-55	$+125$	$^\circ C$
DAC0800LC	0	$+70$	$^\circ C$
DAC0801LC	0	$+70$	$^\circ C$
DAC0802LC	0	$+70$	$^\circ C$

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and I_{OUT} .

Symbol	Parameter	Conditions	DAC0802L/ DAC0802LC			DAC0800L/ DAC0800LC			DAC0801LC			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	8	8	8	Bits
	Nonlinearity				± 0.1			± 0.19			± 0.39	%FS
t_s	Settling Time	To $\pm 1/2$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ C$		100	135					100	150	ns
		DAC0800L				100	135					ns
		DAC0800LC				100	150					ns
t_{PLH} , t_{PHL}	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ C$		35 35	60 60		35 35	60 60		35 35	60 60	ns ns
TC_{FS}	Full Scale Tempco			± 10	± 50		± 10	± 50		± 10	± 80	ppm/ $^\circ C$
V_{OC}	Output Voltage Compliance	Full Scale Current Change $< 1/2$ LSB, $R_{OUT} > 20$ M Ω Typ	-10		18	-10		18	-10		18	V
I_{FS4}	Full Scale Current	$V_{REF} = 10.000V$, $R_{14} = 5.000$ k Ω $R_{15} = 5.000$ k Ω , $T_A = 25^\circ C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
I_{FS5}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		± 0.5	± 4.0		± 1	± 8.0		± 2	± 16	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0		0.2	4.0	μA
I_{FSR}	Output Current Range	$V^- = -5V$ $V^- = -8V$ to $-18V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA mA
V_{IL} , V_{IH}	Logic Input Levels Logic "0" Logic "1"	$V_{LC} = 0V$	2.0		0.8	2.0		0.8	2.0		0.8	V V
I_{IL} , I_{IH}	Logic Input Current Logic "0" Logic "1"	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$ $2V \leq V_{IN} \leq +18V$		-2.0 0.002	-10 10		-2.0 0.002	-10 10		-2.0 0.002	-10 10	μA μA
V_{IS}	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	-10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	-10		13.5	V
I_{15}	Reference Bias Current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dl/dt	Reference Input Slew Rate	(Figure 12)	4.0	8.0		4.0	8.0		4.0	8.0		mA/ μs
PSS_{IFS+}	Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
PSS_{IFS-}		$-4.5V \leq V^- \leq 18V$ $I_{REF} = 1$ mA		0.0001	0.01		0.0001	0.01		0.0001	0.01	%/%
I^+ , I^-	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1$ mA		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8	mA mA
I^+ , I^-		$V_S = 5V$, $-15V$, $I_{REF} = 2$ mA		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	mA mA
I^+ , I^-		$V_S = \pm 15V$, $I_{REF} = 2$ mA		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	mA mA