Integrated Device Technology, Inc.

HIGH-SPEED 4K x 8 DUAL-PORT STATIC RAM

IDT7134SA/LA

FEATURES:

- High-speed access
  - — Military: 25/35/45/55/70ns (max.)
  - — Commercial: 20/25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

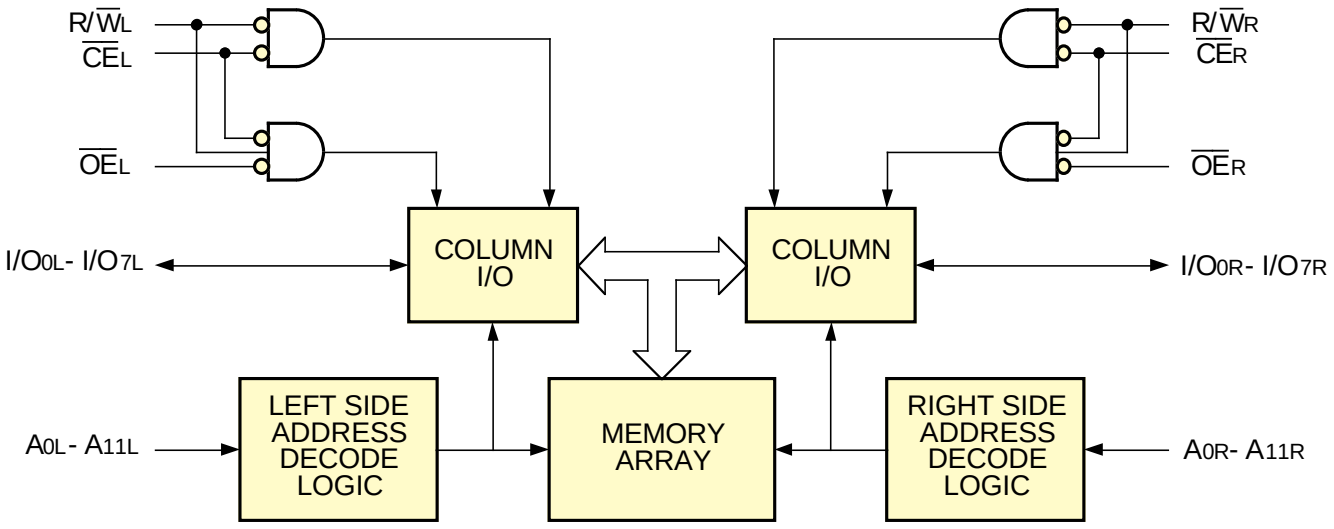
The IDT7134 is a high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these Dual-Port typically on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

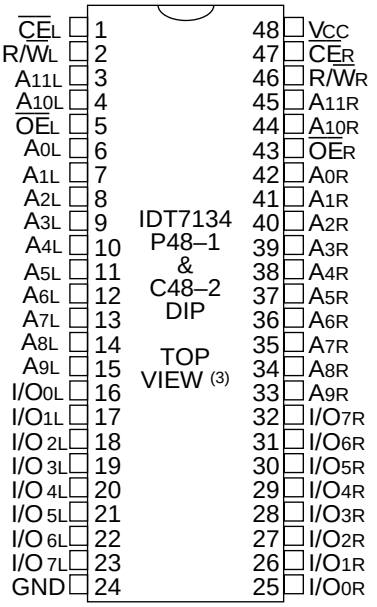
The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Ceramic Flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

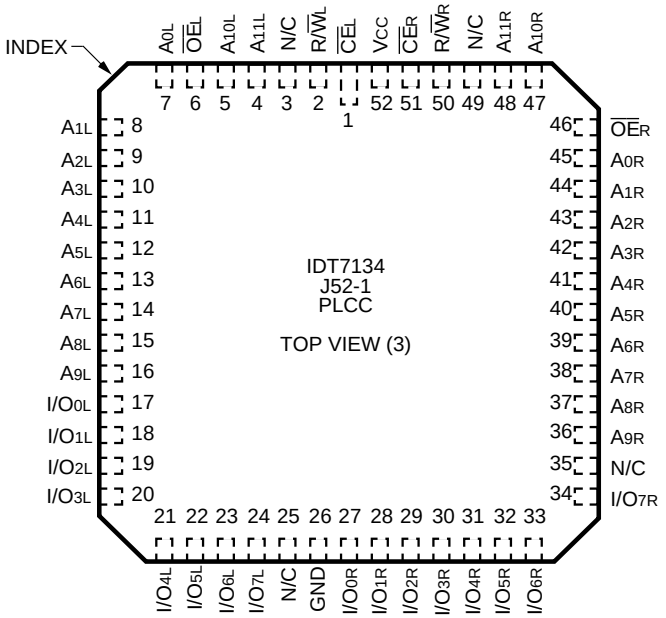


2720 drw 01

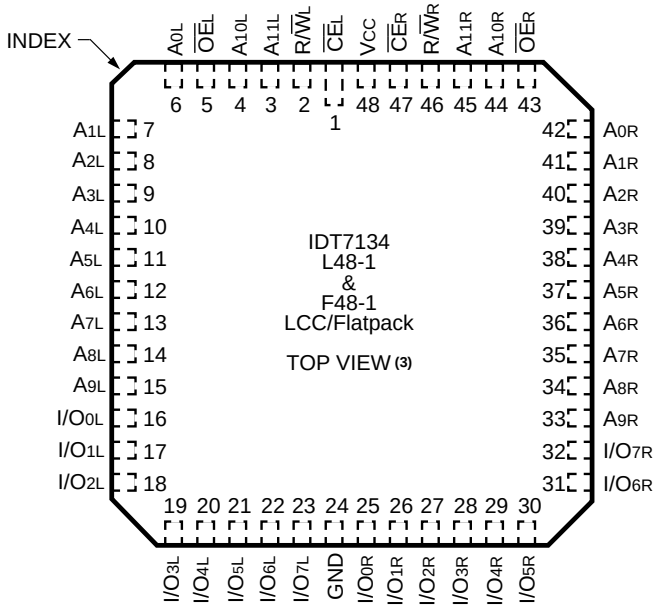
PIN CONFIGURATIONS[1,2]



2720 drw 02



2720 drw 03



2720 drw 04

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T[3]	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

2720 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25%of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc +0.5V.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dv	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dv	11	pF

2720 tbl 02

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2720 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTES:
2720 tbl 04

1. V_{IL} (min.) ≥ –1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134SA		IDT7134LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

NOTE:
2720 tbl 05

1. At Vcc ≤ 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7134X20(4)		7134X25		7134X35		7134X45		7134X55		7134X70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}(3)	MIL.	S	—	—	160	310	150	300	140	280	140	270	140	270	mA
				L	—	—	160	260	150	250	140	240	140	220	140	220	
			COM'L.	S	170	280	160	280	150	260	140	240	140	240	140	240	
				L	170	240	160	220	150	210	140	200	140	200	140	200	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}(3)	MIL.	S	—	—	25	100	25	75	25	70	25	70	25	70	mA
				L	—	—	25	80	25	55	25	50	25	50	25	50	
			COM'L.	S	25	110	25	80	25	75	25	70	25	70	25	70	
				L	25	80	25	50	25	45	25	40	25	40	25	40	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH} Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	—	—	95	210	85	200	75	190	75	180	75	180	mA
				L	—	—	95	170	85	160	75	150	75	150	75	150	
			COM'L.	S	105	180	95	180	85	170	75	160	75	160	75	160	
				L	105	150	95	140	85	130	75	130	75	130	75	130	
I_{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0(3)	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.5	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
I_{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_{"A"}$ or $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}(3)	MIL.	S	—	—	95	210	85	190	75	180	75	170	75	170	mA
				L	—	—	95	150	85	130	75	120	75	120	75	120	
			COM'L.	S	105	170	95	170	85	160	75	150	75	150	75	150	
				L	105	130	95	120	85	110	75	100	75	100	75	100	

NOTES:
2720 tbl 06

1. "X" in part number indicates power rating (SA or LA).
2. V_{CC} = 5V, T_A = +25°C for typical, and parameters are not production tested.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.
4. (Commercial only) 0°C to +70°C temperature range.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

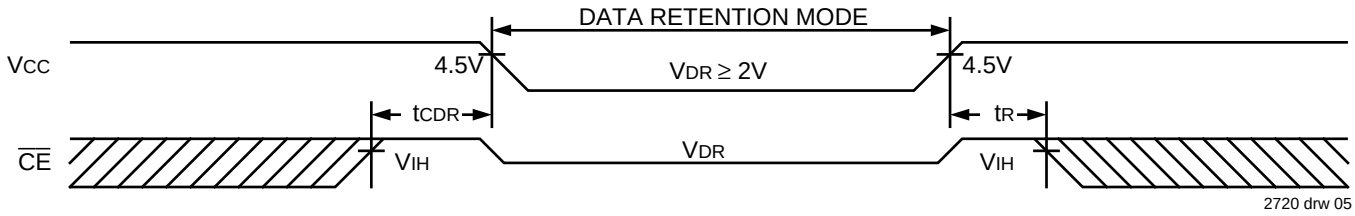
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	VCC for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but not production tested.

2720 tbl 07

DATA RETENTION WAVEFORM

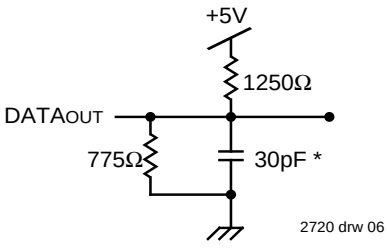


2720 drw 05

AC TEST CONDITIONS

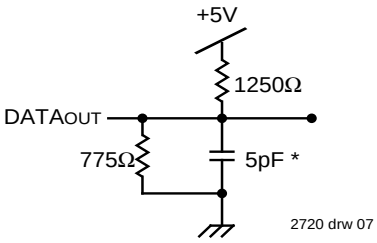
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2720 tbl 08



2720 drw 06

Figure 1. AC Output Test Load



2720 drw 07

Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	7134X20[3]		7134X25		7134X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

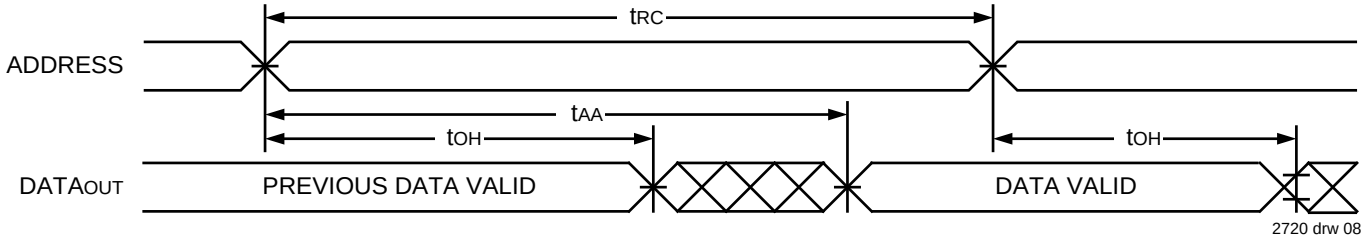
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4] (CONT'D)

Symbol	Parameter	7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	45	—	50	—	50	ns

NOTES:
2720 tbl 09

1. Transition is measured ±500mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. (Commercial only) 0°C to +70°C temperature range only.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 3]

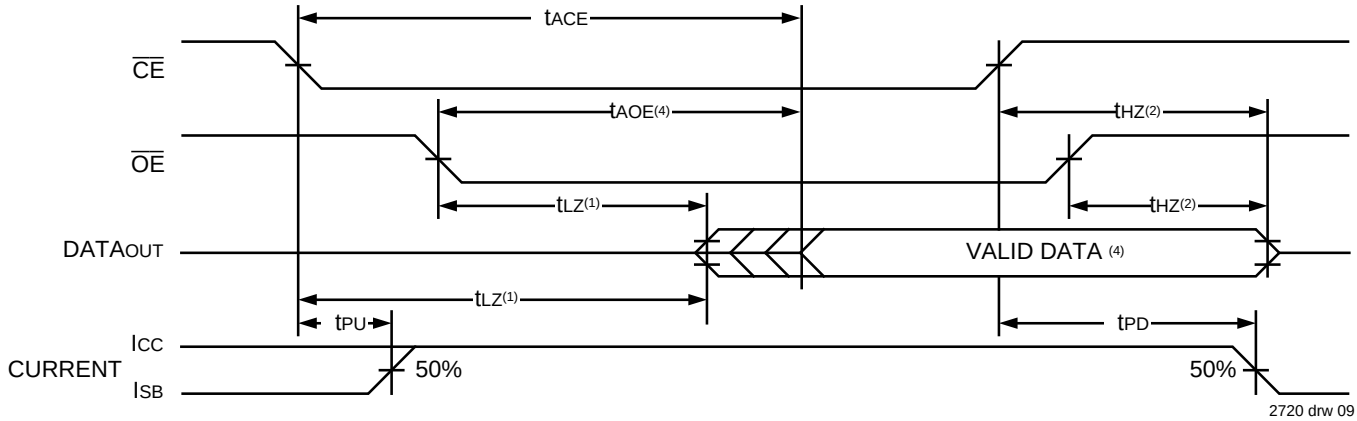


2720 drw 08

NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH}.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1, 3)



2720 drw 09

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = V_{IH}.
4. Start of valid data depends on which timing becomes effective , t_{AOE}, t_{ACE} or t_{AA}
5. t_{AA} for RAM Address Access and t_{SAA} for Semaphore Address Access.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	7134X20(5)		7134X25		7134X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write RecoveryTime	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time(1, 2)	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time(3)	0	—	0	—	3	—	ns
t_{WZ}	Write Enabled to Output in High-Z(1, 2)	—	15	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write(1, 2, 3)	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay(4)	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(4, 7)	—	30	—	30	—	35	ns

NOTES: 2720 tbl 10

1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read”.
5. (Commercial only), 0°C to +70°C temperature range .
6. “X” in part number indicates power rating (SA or LA).
7. t_{DDD} = 35ns for military temperature range.

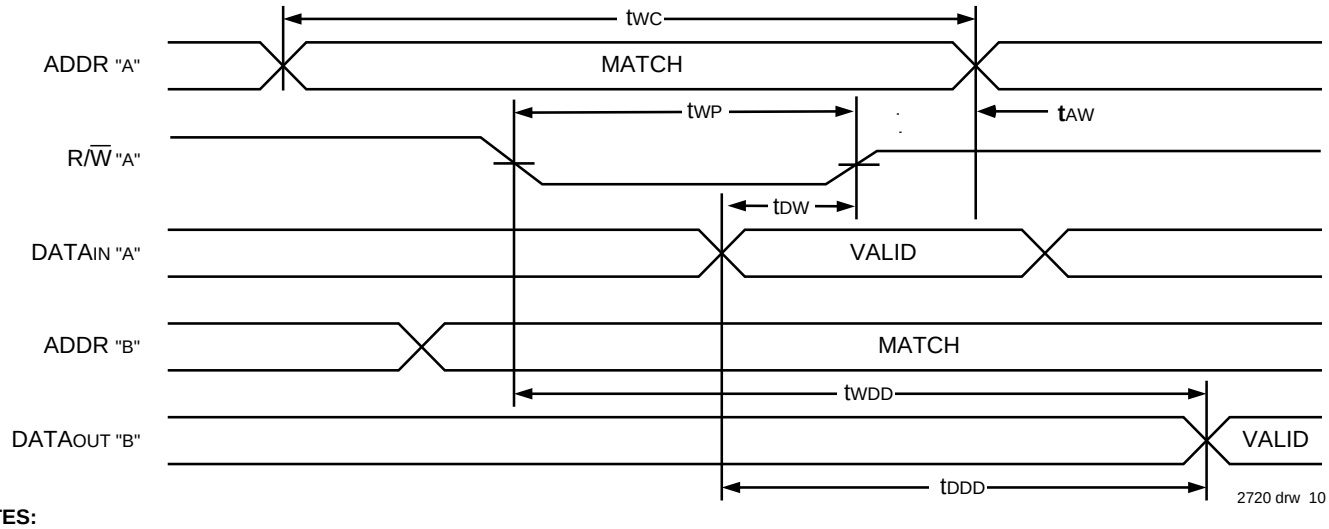
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[6] (CONT'D)

Symbol	Parameter	7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write RecoveryTime	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[3]	3	—	3	—	3	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	20	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1, 2, 3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	45	—	55	—	70	ns

2720 tbl 10

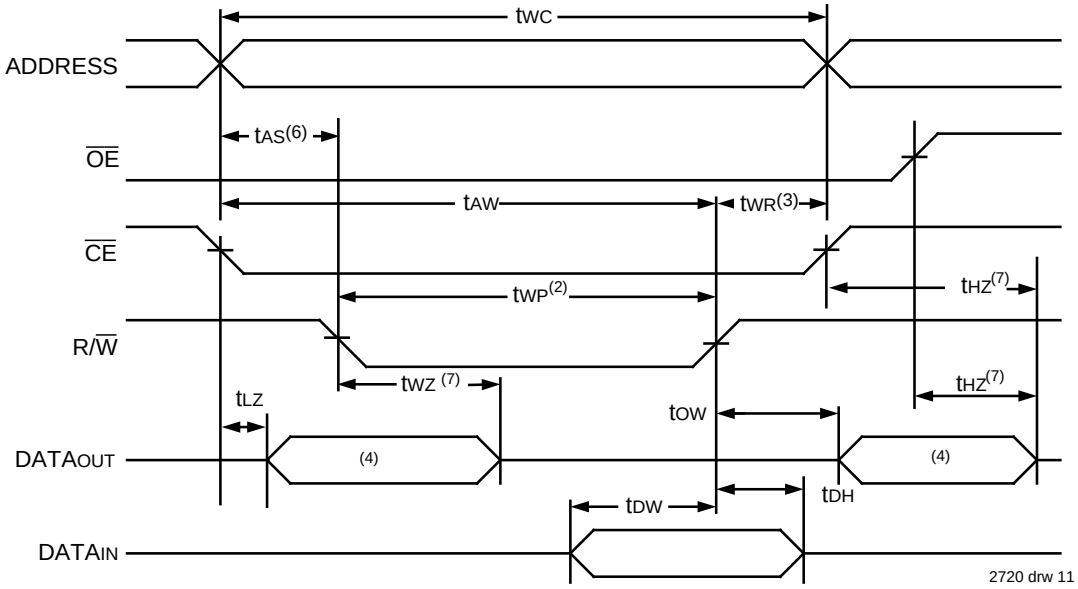
NOTES:
1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Write with Port-to-Port Read”.
5. (Commercial only), 0°C to +70°C temperature range .
6. “X” in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ [1]

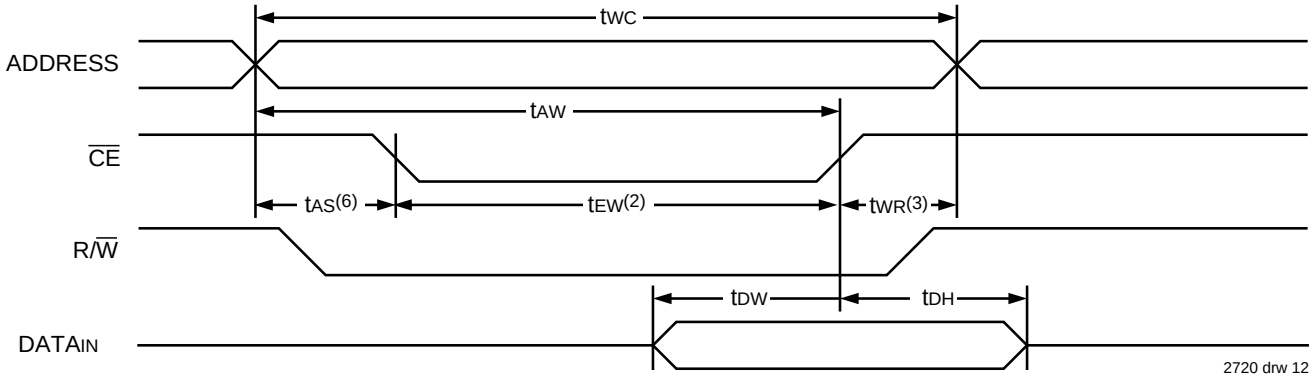


NOTES:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$. $\overline{OE}_{"B"} = V_{IL}$.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 5, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ =V_{IL} and R/$\overline{W}$ = V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$)is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

FUNCTIONAL DESCRIPTION

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

TRUTH TABLE I – READ/WRITE CONTROL(2)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on port written into memory
H	L	L	$DATA_{OUT}$	Data in memory output on port
X	X	H	Z	High impedance outputs

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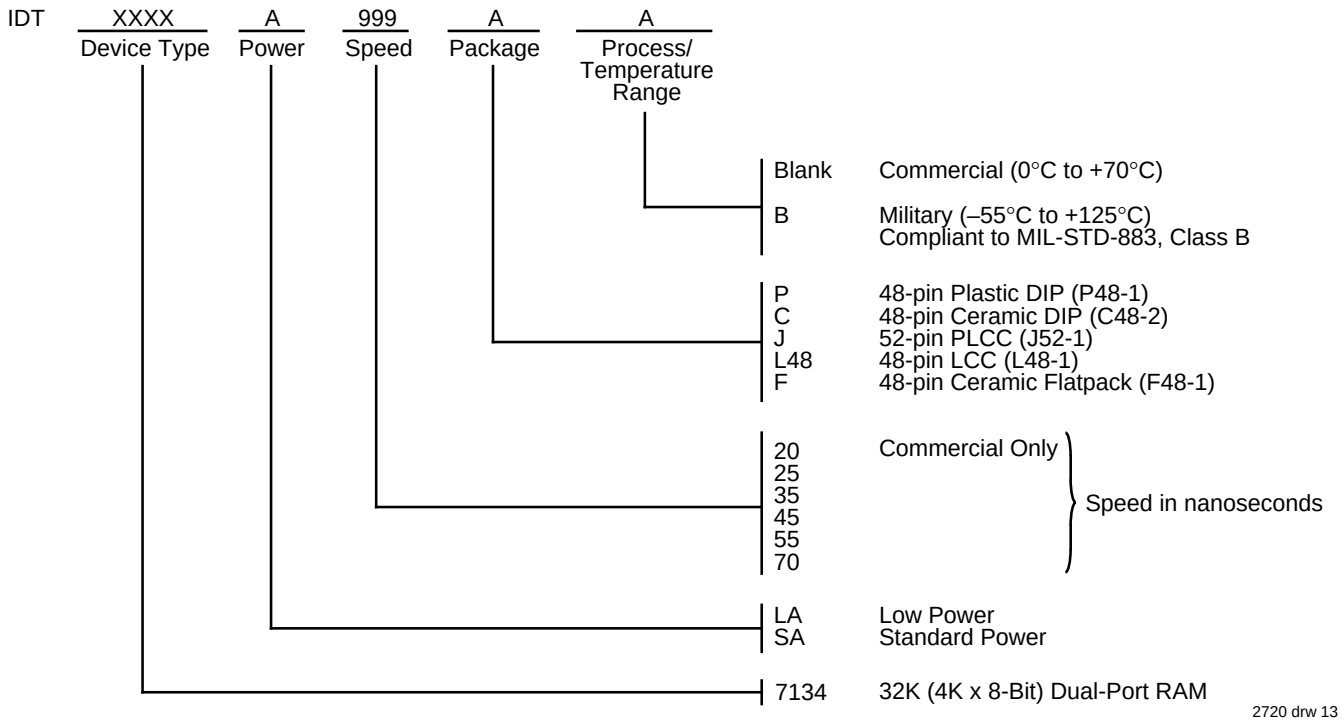
NOTES:
1. A_{OL} - $A_{11L} \neq A_{OR}$ - A_{11R}
2. "H" = HIGH, "L" = LOW, "X" = Don't Care, and "Z" = High-impedance

ORDERING INFORMATION



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